United States Patent [19]

Raymond et al.

[11] **4,216,539**

[45] **Aug. 5, 1980**

[54] IN-CIRCUIT DIGITAL TESTER

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[73] Assignee: **Zehntel, Inc., Concord, Calif.**

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[51] **Int. Cl.²** **G01R 31/28; G06F 11/00**

[52] **U.S. Cl.** ..... **371/20; 324/73 R**

[58] **Field of Search** ..... 235/302; 324/73 R, 73 AT, 324/73 PC; 364/200, 900; 371/15, 20

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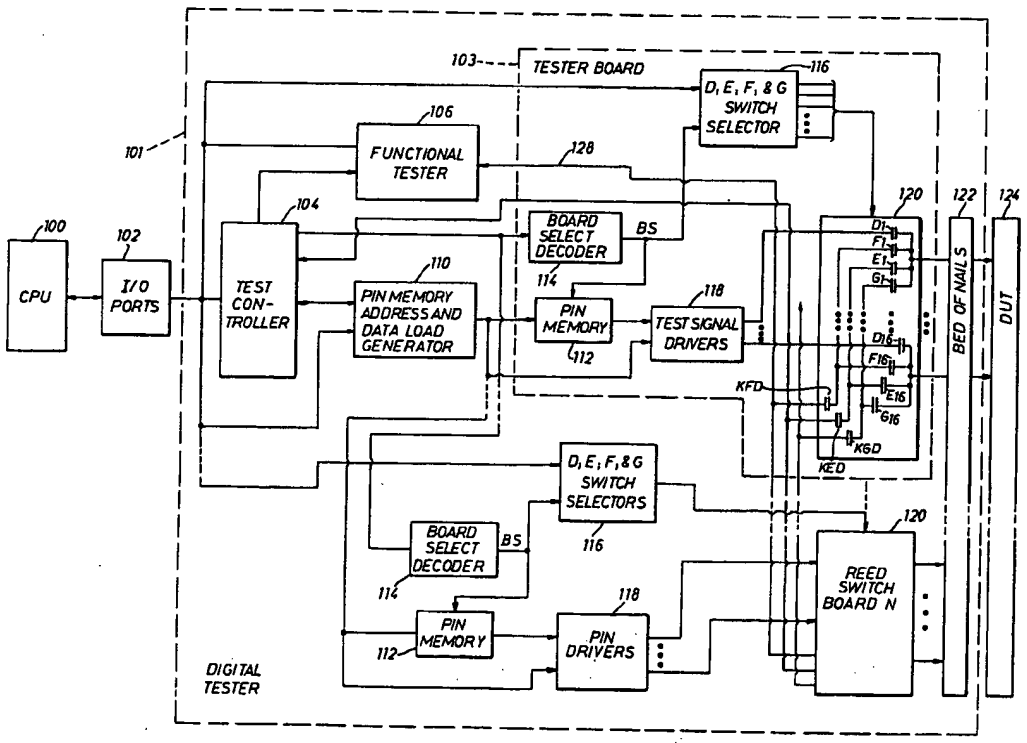
Primary Examiner—Charles E. Atkinson

Attorney, Agent, or Firm—Arnold, White & Durkee

[57] **ABSTRACT**

An apparatus for the automatic, in-circuit testing of the electrical properties of complex digital integrated circuit assemblies is disclosed. A programmed processor is provided to control a set of selectable switches, which connect selected nodes of a circuit under test to certain ones of a plurality of signal lines. One of the signal lines supplies a selected digital test signal from a set of selectable test signals to the selected node. The set of test signals including a Gray code. Another of the signal lines provides a response line connecting a selected node to a functional tester that performs one of a selectable number of intermediate functional tests. One of the functional tests is a signature analysis of the digital response signal in accordance with a cyclic redundancy check (CRC) coding technique. Each test performed by the apparatus is specified through processor routines which select and encode the proper test signals for the particular circuit or device under test and analyze the results of the intermediate functional tests to determine if the device has functioned properly.

60 Claims, 11 Drawing Figures



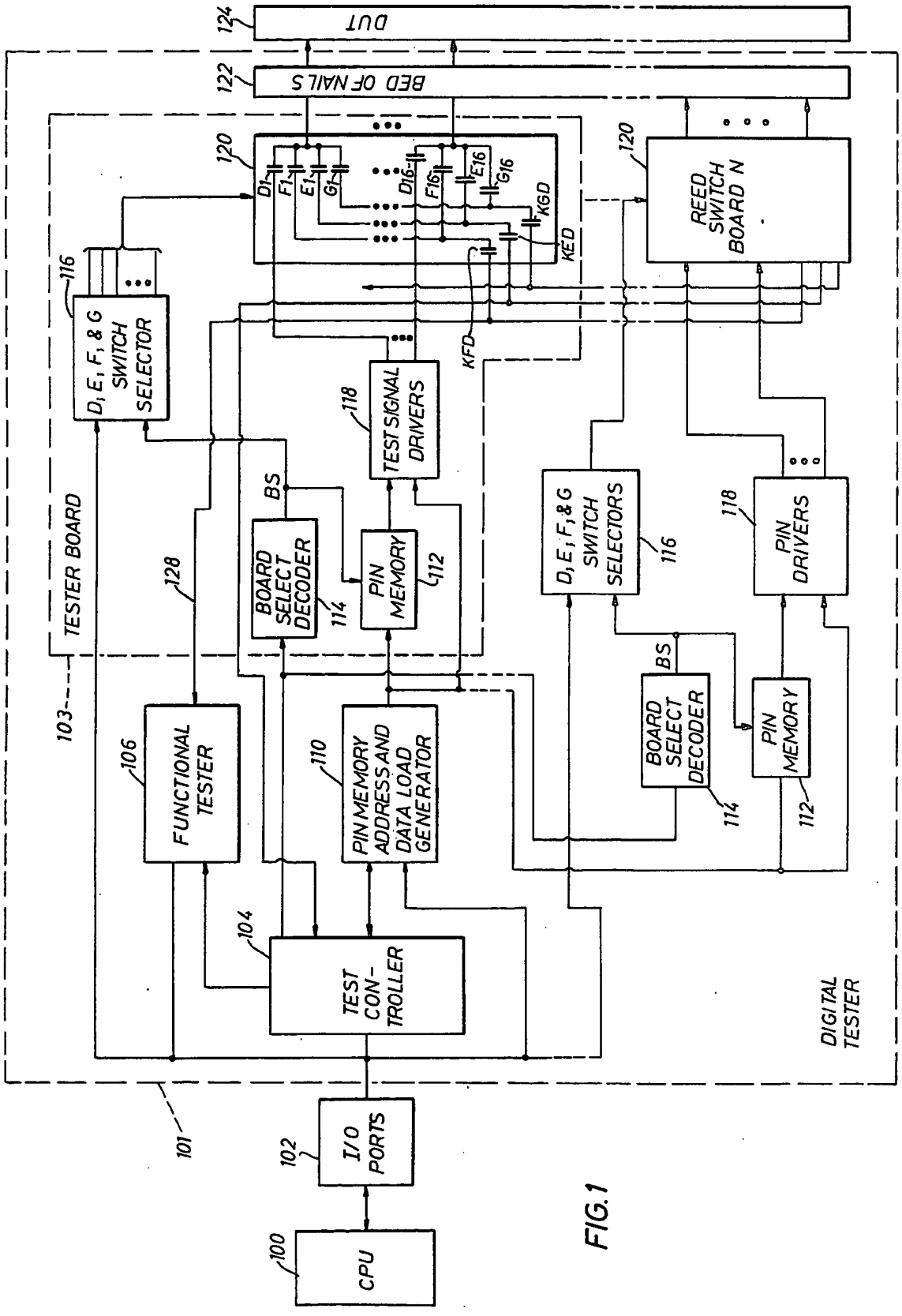

DUT
124
BED OF NAILS
122
120
D1
F1
E1
G1
D16
F16
E16
G16
KGD
KED
KFD
REED SWITCH BOARD N
120
116
D, E, F, & G SWITCH SELECTOR
118
TEST SIGNAL DRIVERS
BS
BOARD SELECT DECODER
114
PIN MEMORY
112
128
TESTER BOARD
103
D, E, F, & G SWITCH SELECTORS
116
118
PIN DRIVERS
BS
BOARD SELECT DECODER
114
PIN MEMORY
112
106
FUNCTIONAL TESTER
110
PIN MEMORY ADDRESS AND DATA LOAD GENERATOR
104
TEST CON-TROLLER
DIGITAL TESTER
101
102
I/O PORTS
100
CPU

FIG. 1

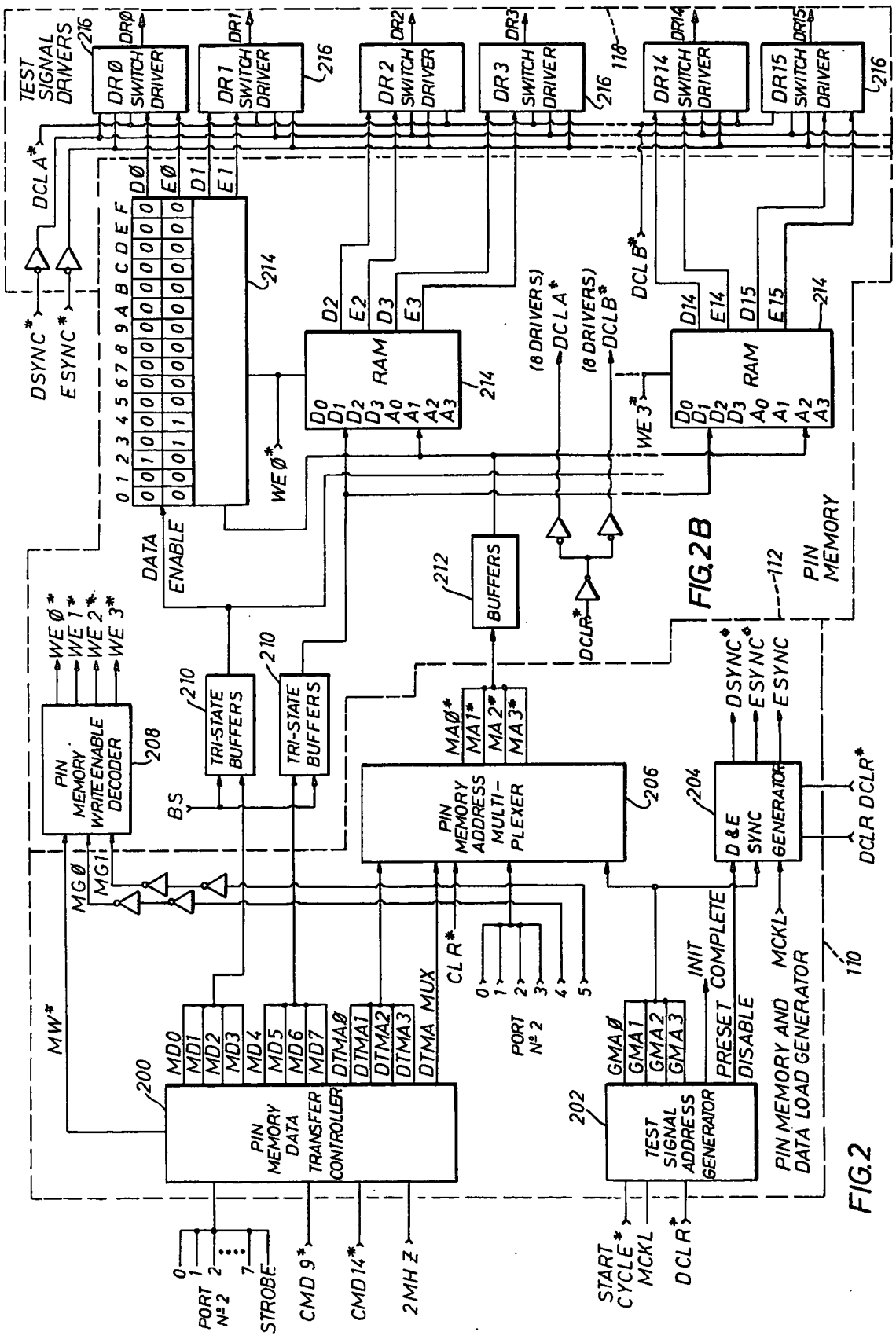

TEST SIGNAL DRIVERS
DR Ø SWITCH DRIVER
DR 1 SWITCH DRIVER
DR 2 SWITCH DRIVER
DR 3 SWITCH DRIVER
DR14 SWITCH DRIVER
DR15 SWITCH DRIVER
DCL A*
DCL B*
DSYNC*
ESYNC*
RAM
WE Ø*
WE 3*
(8 DRIVERS) DCL A*
(8 DRIVERS) DCL B*
DATA ENABLE
BUFFERS
DCLR*
PIN MEMORY
WE Ø* WE 1* WE 2* WE 3*
PIN MEMORY WRITE ENABLE DECODER
TRI-STATE BUFFERS
BS
MAØ* MA1* MA2* MA3*
PIN MEMORY ADDRESS MULTI-PLEXER
D & E SYNC GENERATOR
DCLR DCLR*
MGØ MG1
MW*
MDØ MD1 MD2 MD3 MD4 MD5 MD6 MD7
DTMAØ DTMA1 DTMA2 DTMA3 DTMA MUX
CLR*
PORT Nº 2
GMAØ GMA1 GMA2 GMA3
INIT PRESET DISABLE
COMPLETE
MCKL
PIN MEMORY DATA TRANSFER CONTROLLER
TEST SIGNAL ADDRESS GENERATOR
PIN MEMORY AND DATA LOAD GENERATOR
PORT Nº 2
STROBE
CMD 9*
CMD 14*
2MHZ
START CYCLE*
MCKL
DCLR*

FIG.2B

FIG.2

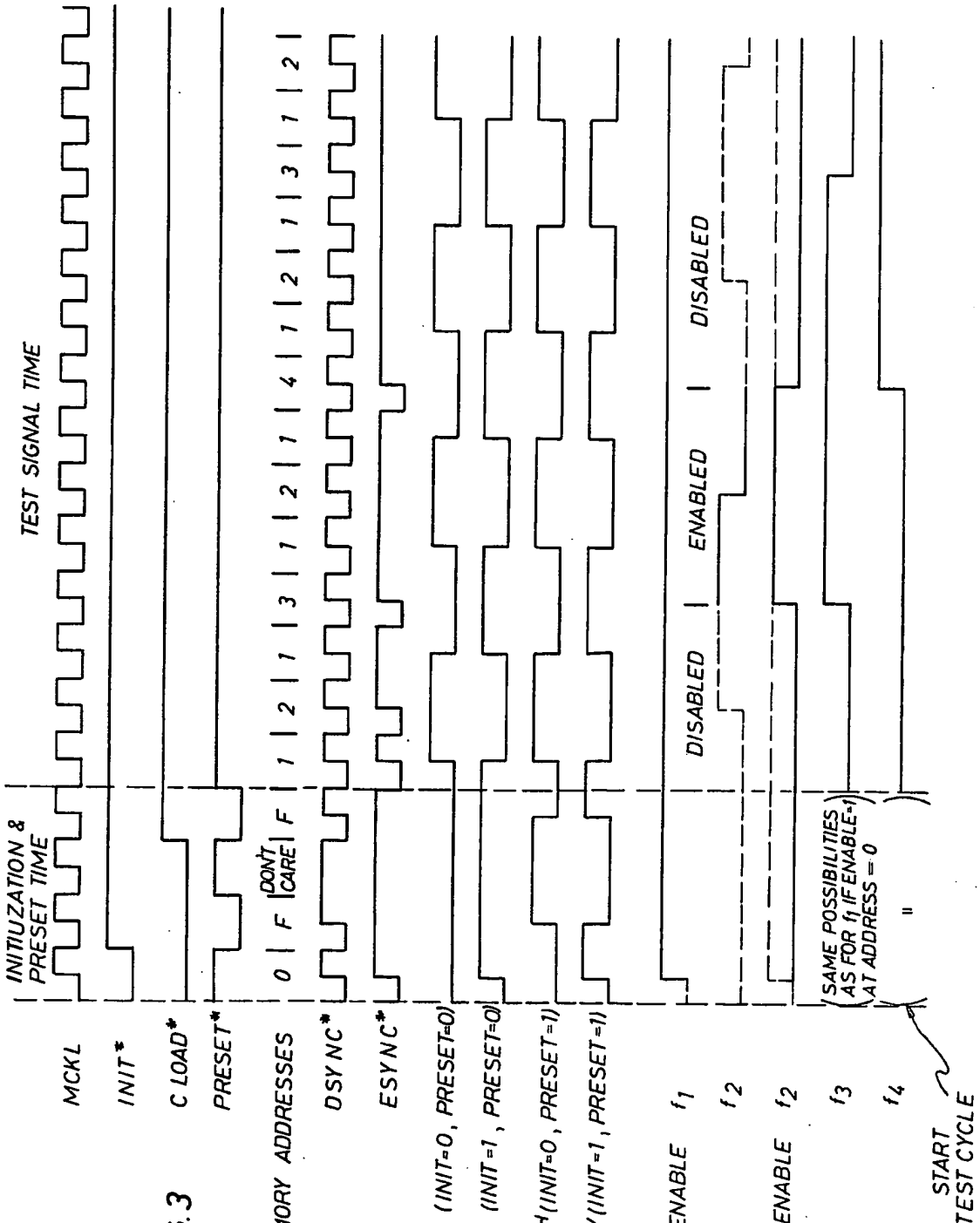

INITIUZATION & PRESET TIME
TEST SIGNAL TIME
MCKL
INIT*
C LOAD*
PRESET*
PIN MEMORY ADDRESSES
0 | F | DON'T CARE | F | 1 | 2 | 1 | 3 | 1 | 2 | 1 | 4 | 1 | 2 | 1 | 3 | 1 | 2 |
DSYNC*
ESYNC*
f1 (INIT=0, PRESET=0)
f1* (INIT=1, PRESET=0)
PRESET HIGH f1 (INIT=0, PRESET=1)
PRESET LOW f1* (INIT=1, PRESET=1)
DRIVE ENABLE f1
DISABLED
ENABLED
DISABLED
f2
DRIVE ENABLE f2
f3
f4
SAME POSSIBILITIES AS FOR f1 IF ENABLE=1 AT ADDRESS = 0
START TEST CYCLE

FIG. 3

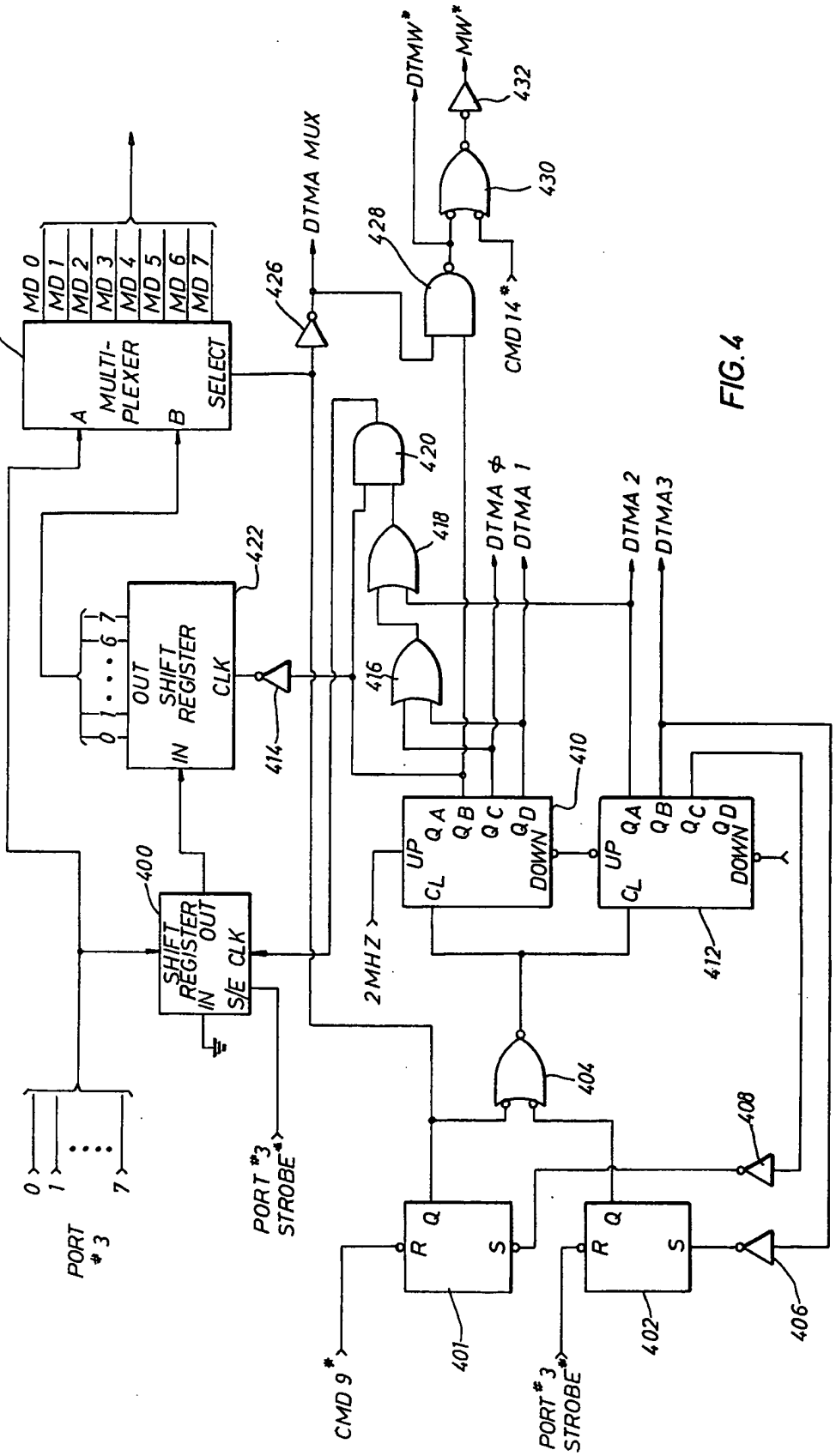
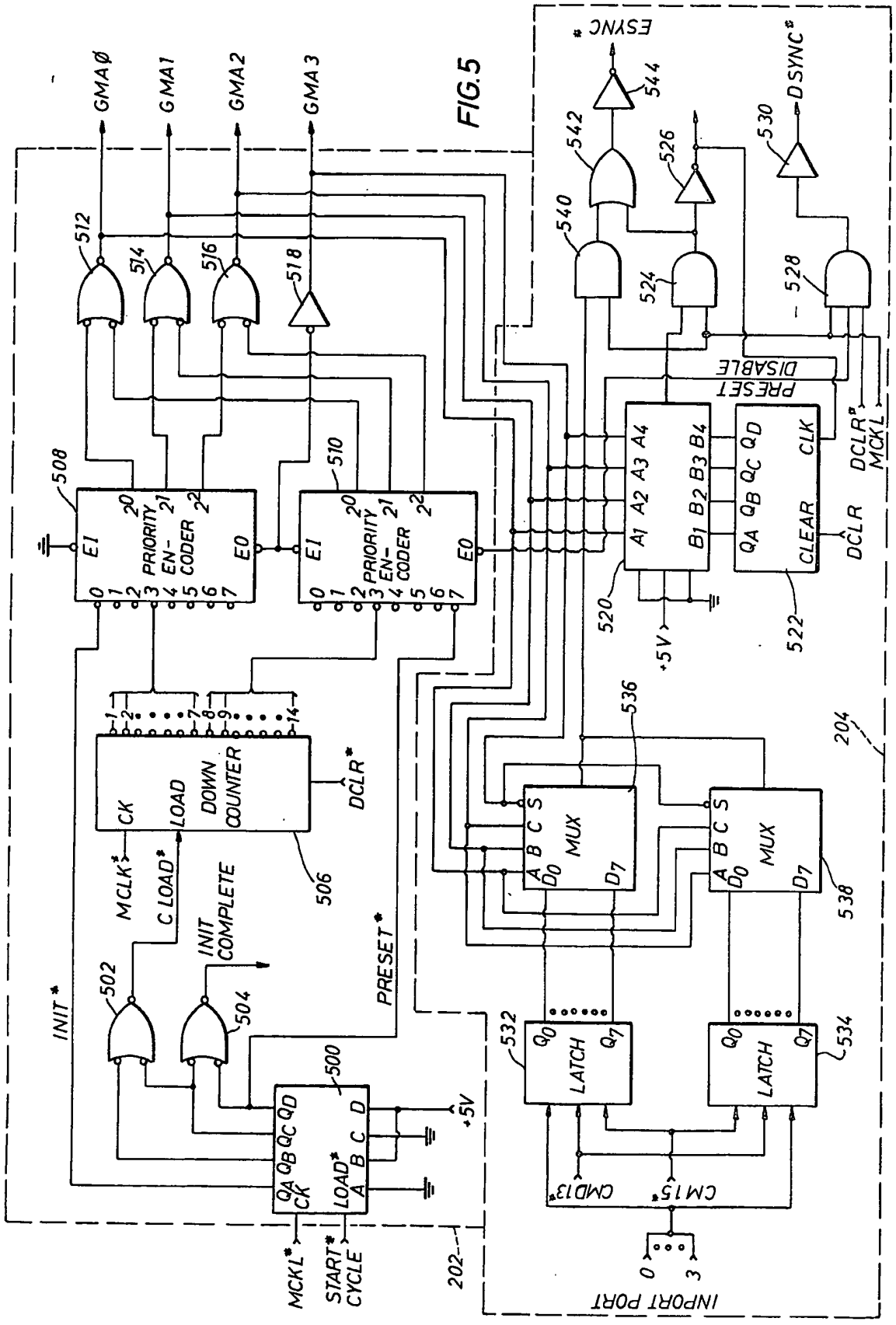

DTMW*
MW*
432
430
428
426
DTMA MUX
CMD 14*
424
MD 0
MD 1
MD 2
MD 3
MD 4
MD 5
MD 6
MD 7
MULTI-PLEXER
A
B
SELECT
420
418
416
DTMA 0
DTMA 1
DTMA 2
DTMA3
422
OUT
SHIFT REGISTER
CLK
IN
414
410
UP
DOWN
QA
QB
QC
QD
CL
400
SHIFT REGISTER
IN
OUT
S/E
CLK
2MHZ
412
404
408
406
R
S
Q
401
402
CMD 9*
PORT #3 STROBE*
PORT #3
0
1
7

FIG. 4

FIG. 5


GMA Ø
GMA 1
GMA 2
GMA 3
ESYNC*
DSYNC*
544
542
526
530
540
524
528
512
514
516
518
508
510
PRIORITY EN-CODER
E1
E0
0 1 2 3 4 5 6 7
20 21 22
DISABLE
PRESET
DCLR*
MCKL
A1 A2 A3 A4
B1 B2 B3 B4
QA QB QC QD
CLK
CLEAR
520
522
+5V
536
204
DOWN COUNTER
CK
LOAD
506
MCLK*
C LOAD*
INIT COMPLETE
INIT*
PRESET*
502
504
500
MUX
A B C S
D0 D7
538
LATCH
Q0 Q7
532
534
CM15*
CM13*
INPORT PORT
0 3
MCKL*
START* CYCLE
202

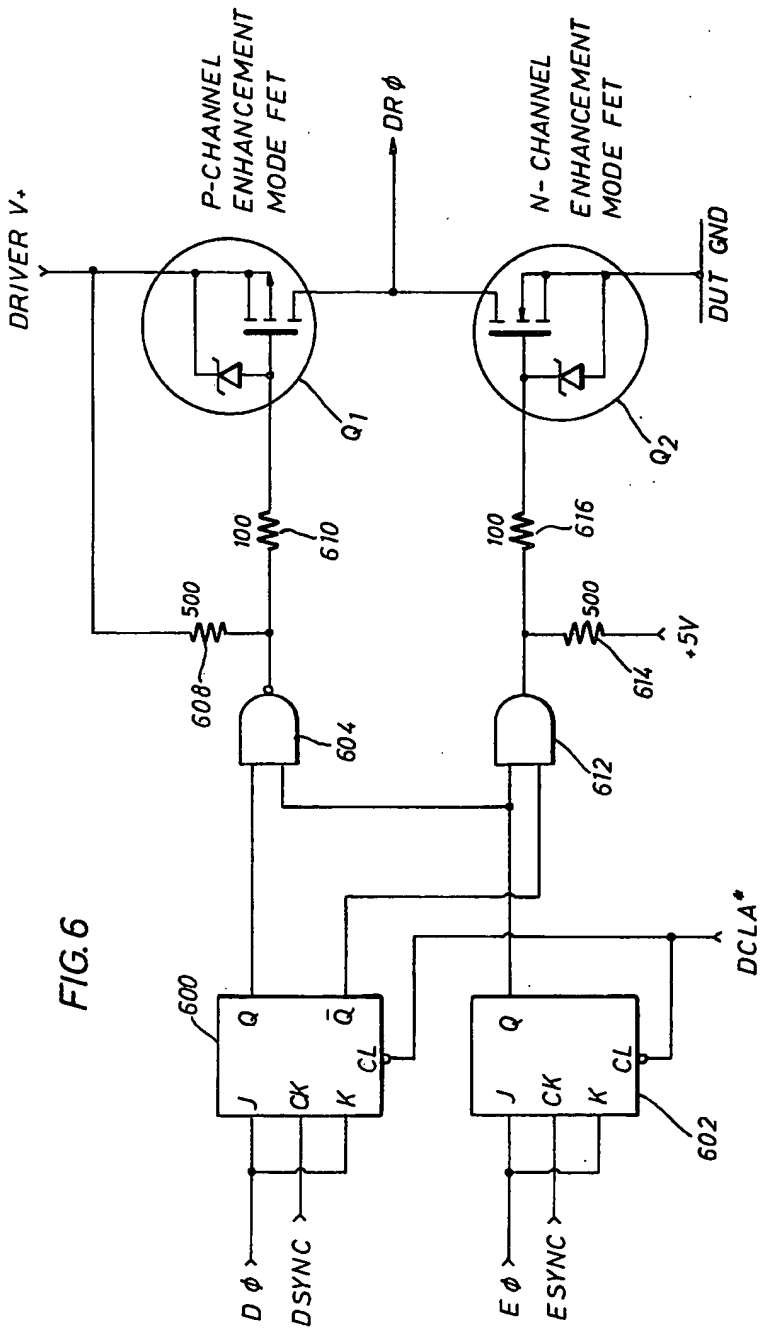

P-CHANNEL ENHANCEMENT MODE FET
N-CHANNEL ENHANCEMENT MODE FET
DR ϕ
DRIVER V+
DUT GND
Q1
Q2
100
610
100
616
500
608
500
614
+5V
604
612
DCLA*
600
602
Q
Q̄
CL
J
CK
K
D ϕ
DSYNC
E ϕ
ESYNC

FIG. 6

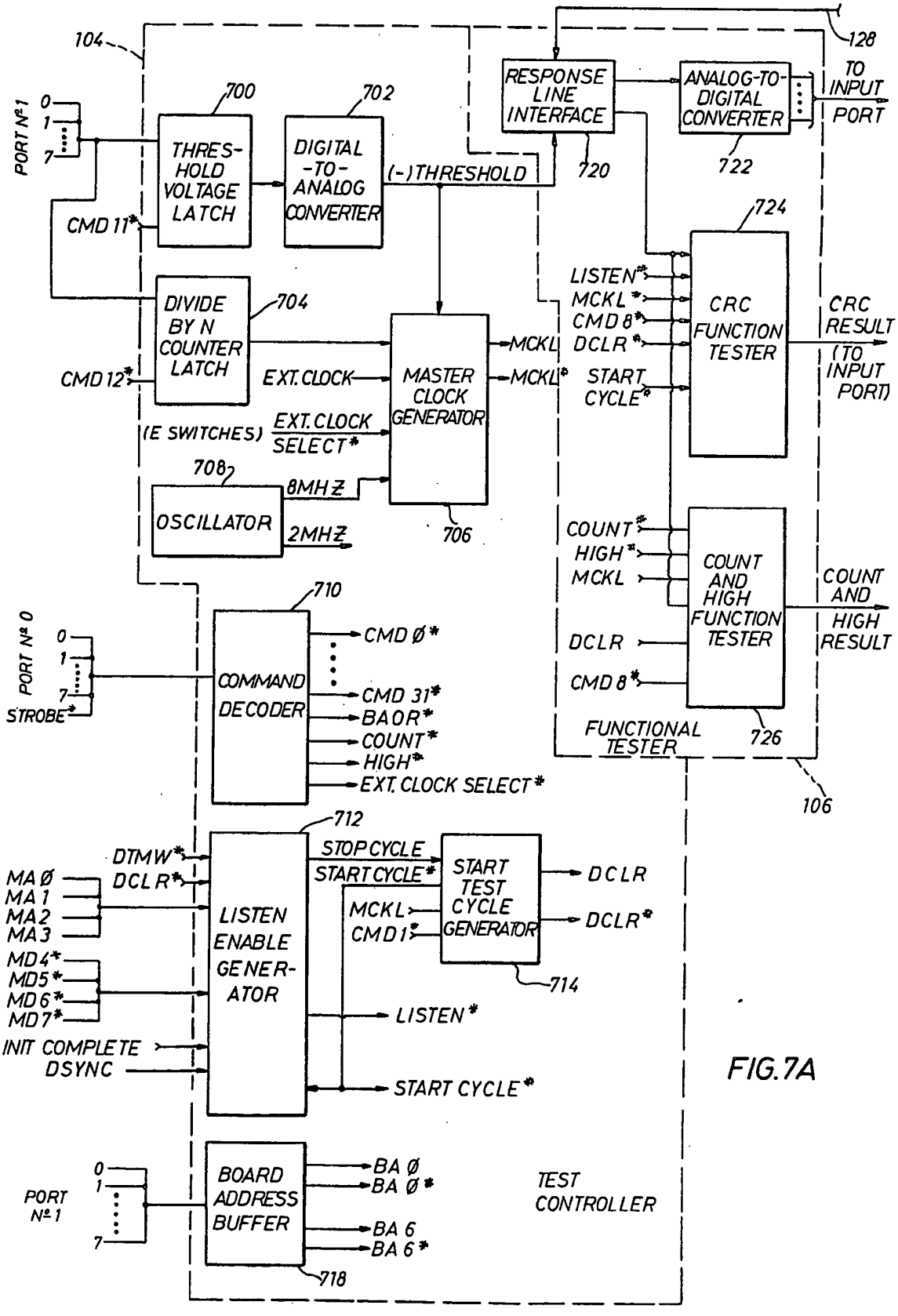

104
128
RESPONSE LINE INTERFACE
ANALOG-TO-DIGITAL CONVERTER
TO INPUT PORT
PORT Nº1
0
1
7
700
THRES-HOLD VOLTAGE LATCH
702
DIGITAL -TO- ANALOG CONVERTER
(-)THRESHOLD
720
722
CMD 11*
724
LISTEN*
MCKL*
CMD 8*
DCLR*
CRC FUNCTION TESTER
CRC RESULT (TO INPUT PORT)
DIVIDE BY N COUNTER LATCH
704
CMD 12*
EXT. CLOCK
MASTER CLOCK GENERATOR
MCKL
MCKL*
START CYCLE*
(E SWITCHES) EXT. CLOCK SELECT*
708
8MHZ
OSCILLATOR
2MHZ
706
COUNT*
HIGH*
MCKL
COUNT AND HIGH FUNCTION TESTER
COUNT AND HIGH RESULT
DCLR
CMD 8*
FUNCTIONAL TESTER
726
106
710
PORT Nº 0
0
1
7
STROBE*
COMMAND DECODER
CMD Ø*
CMD 31*
BAOR*
COUNT*
HIGH*
EXT. CLOCK SELECT*
712
DTMW*
DCLR*
MA Ø
MA 1
MA 2
MA 3
MD4*
MD5*
MD6*
MD7*
INIT COMPLETE
DSYNC
LISTEN ENABLE GENER-ATOR
STOP CYCLE
START CYCLE*
START TEST CYCLE GENERATOR
MCKL
CMD 1*
DCLR
DCLR*
714
LISTEN*
START CYCLE*
PORT Nº1
0
1
7
BOARD ADDRESS BUFFER
BA Ø
BA Ø*
BA 6
BA 6*
718
TEST CONTROLLER

FIG. 7A

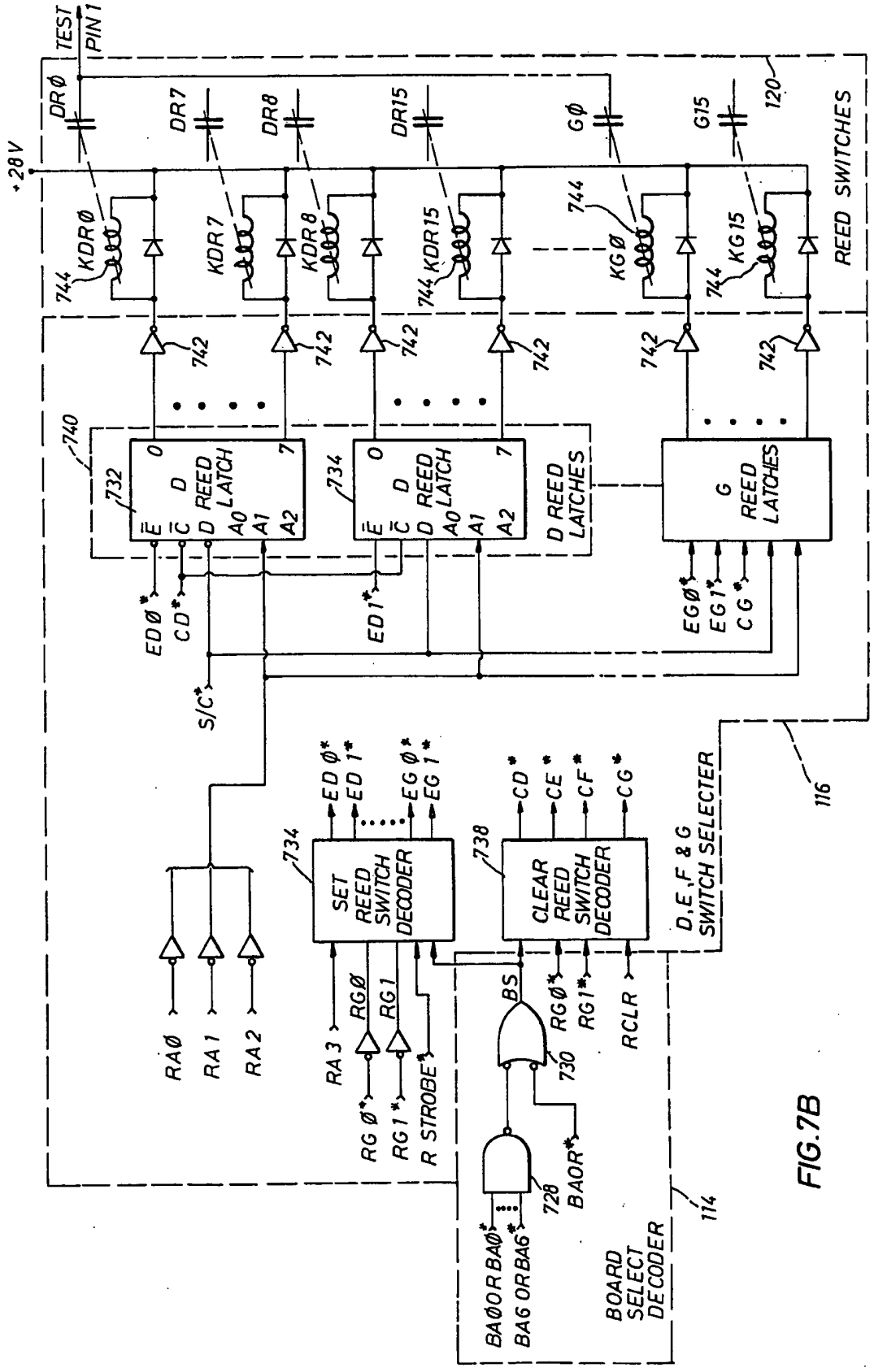

TEST PIN 1
+28V
DRØ
DR7
DR8
DR15
GØ
G15
120
REED SWITCHES
KDRØ
KDR7
KDR8
KDR15
KGØ
KG15
744
742
740
732
734
D REED LATCH
D REED LATCHES
G REED LATCHES
EDØ*
CD*
S/C*
ED1*
EGØ*
EG1*
CG*
116
SET REED SWITCH DECODER
CLEAR REED SWITCH DECODER
738
D,E,F & G SWITCH SELECTER
RAØ
RA1
RA2
RA3
RGØ
RG1
R STROBE*
RG Ø*
RG 1*
BS
730
RCLR
728
BAOR*
BAØ OR BA4*
BA3 OR BA6*
BOARD SELECT DECODER
114

FIG.7B

FIG. 8

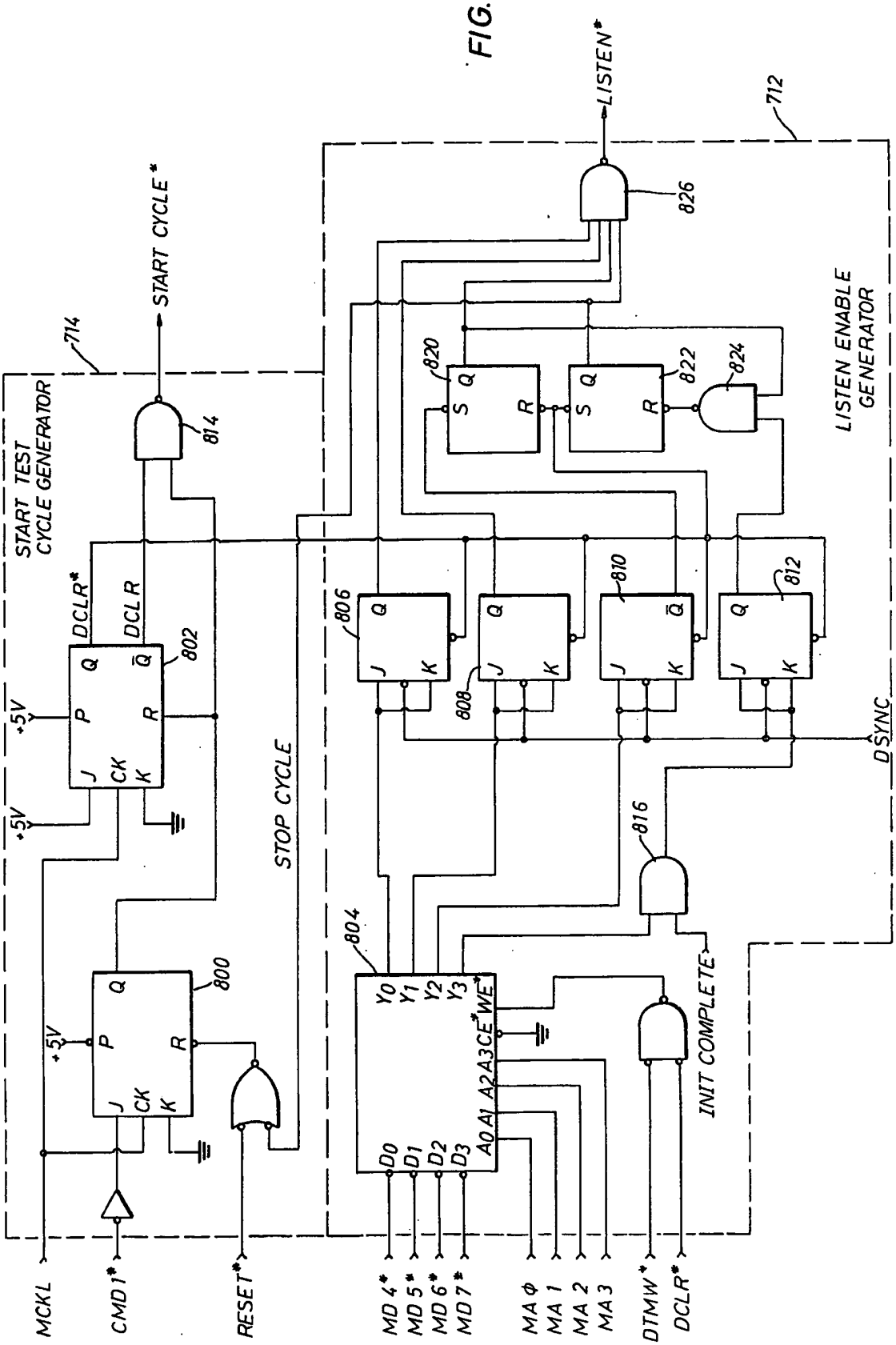
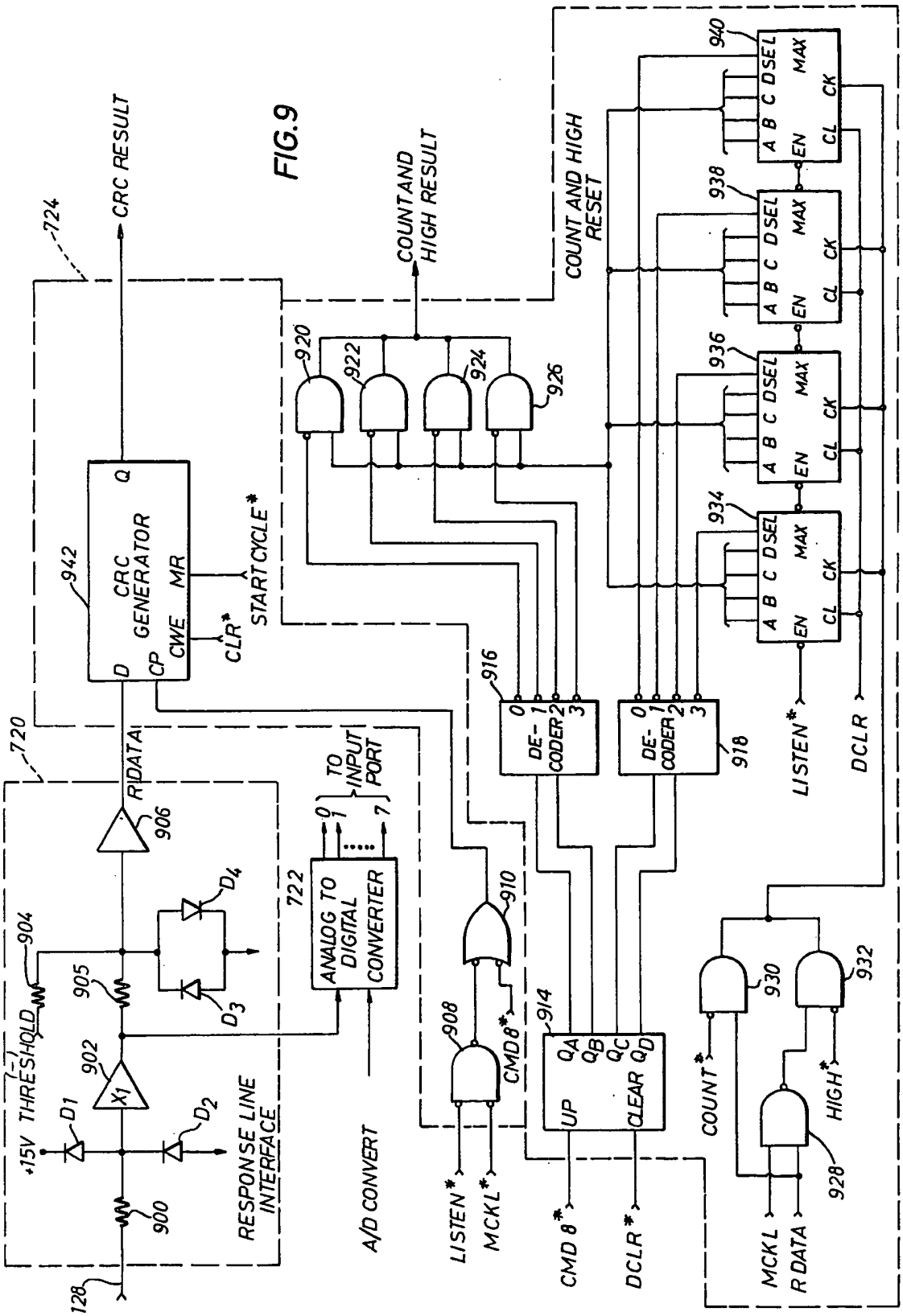

LISTEN*
712
826
START CYCLE*
714
START TEST CYCLE GENERATOR
814
820
822
824
LISTEN ENABLE GENERATOR
DCLR*
DCLR
802
806
808
810
812
+5V
DSYNC
STOP CYCLE
816
804
800
INIT COMPLETE
MCKL
CMD1*
RESET*
MD 4*
MD 5*
MD 6*
MD 7*
MA Φ
MA 1
MA 2
MA 3
DTMW*
DCLR*

FIG. 9


CRC RESULT
724
COUNT AND HIGH RESULT
COUNT AND HIGH RESET
940
938
936
934
A B C DSEL MAX
EN CL CK
920
922
924
926
Q
CRC GENERATOR
D CP CWE MR
942
START CYCLE*
CLR*
916
DE-CODER 0 1 2 3
918
720
RDATA
906
TO INPUT PORT
0 1 7
722
ANALOG TO DIGITAL CONVERTER
910
904
905
902
X1
D1
D2
D3
D4
+15V THRESHOLD
900
128
RESPONSE LINE INTERFACE
A/D CONVERT
908
CMD 8*
914
QA QB QC QD
UP CLEAR
LISTEN*
MCKL*
CMD 8*
DCLR*
LISTEN*
DCLR
930
932
COUNT*
HIGH*
928
MCKL
R DATA

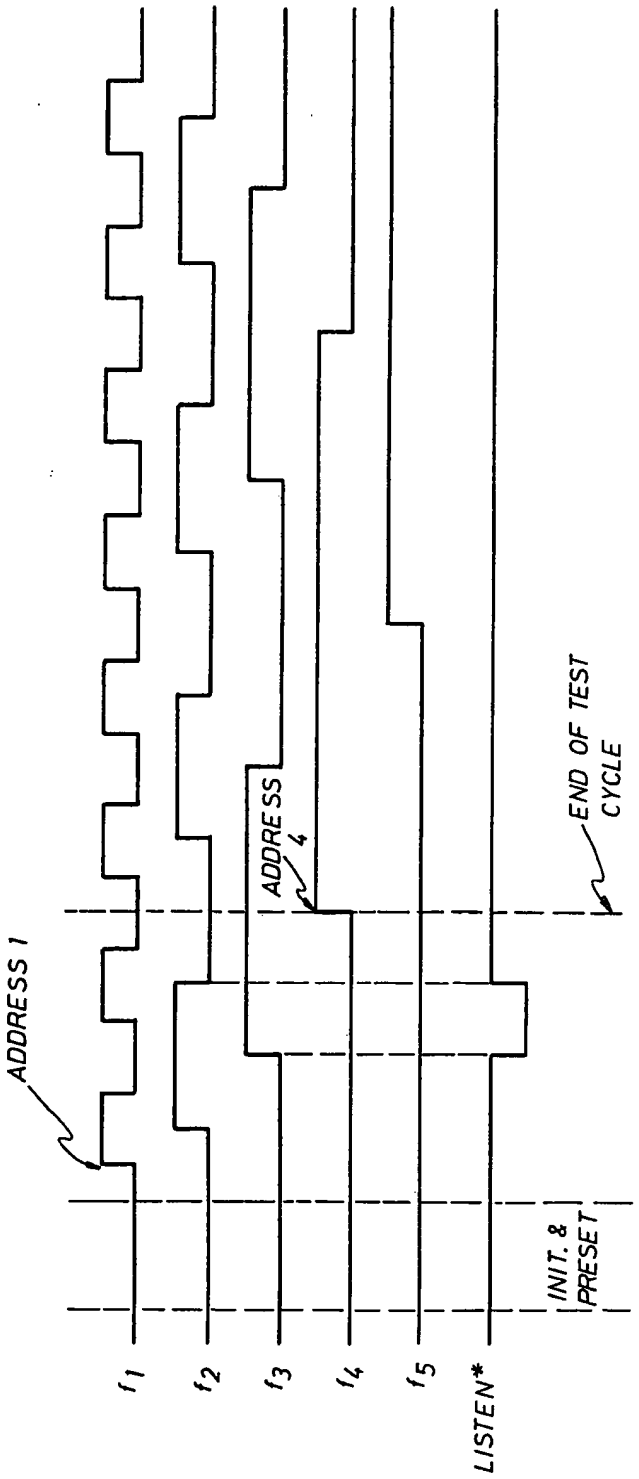

ADDRESS 1
ADDRESS 4
END OF TEST CYCLE
INIT. & PRESET
t_1
t_2
t_3
t_4
t_5
LISTEN*

FIG. 10

IN-CIRCUIT DIGITAL TESTER

BACKGROUND OF THE INVENTION

The present invention relates to a measuring and testing apparatus for testing complex digital circuits; more particularly, to automatic digital in-circuit testers for testing digital circuits containing, but not limited to, large scale integrated circuits.

The in-circuit tester of the type disclosed herein is a tester that is capable of testing a circuit without regard to whether or not the electrical node into which a test signal is injected is connected to the output of another logic device. The disclosed in-circuit tester is capable of generating and applying a digital test signal to an output node of a logic device that is normally at a logic ground, and cause that output to go to a logic high without damaging the device. In other words, the use of the term "in-circuit" means that the device or circuit under test does not have to be isolated or removed from the surrounding circuits in order to apply test signals and to monitor its output.

Printed circuit boards containing complex digital integrated logic circuits interconnected by copper lands to form functional circuits, offer a greater challenge to prior-art in-circuit digital testers than they are able to meet. Prior art testers are able to select interconnection points between the digital components, referred to as the electrical nodes, and to apply test signals to a circuit or to monitor the response of the circuit to those signals. However, ever-increasing complex logic devices, such as micro-processors, are being developed and extensively used by today's circuit designers. Prior-art digital in-circuit testers are not capable of performing the numerous, rapid and varied tests required for such complex circuits.

One of the most significant developments in digital circuit technology in recent years has been the fabrication of large and complex digital circuits on a single chip of semiconductor material using large scale integration (LSI) techniques. These circuits typically contain a great number of transistors and other components which enable the designer to package a greater number of circuits in a relatively small volume. Research and development is underway in the form of very large scale integration (VLSI) for methods to manufacture an even greater number of circuits within a single chip. Where LSI has thousands of transistors per chip, VLSI has hundreds of thousands. As a result of the large number of circuits contained in LSI devices and the expected increases in circuit complexity from VLSI technology, the probability of chip failure has increased. Correspondingly, the importance of testing and diagnosis of chip failures has also increased. However, the prior-art digital in-circuit testers either are not capable of performing the complex tests required, or are too slow, due to the time required to generate all the necessary test signals to test these complex circuits.

Because of the increased packing density of digital circuits and the wide variety of logic functions available, LSI devices are enjoying widespread use in most digital circuits and systems which designers are presently producing. The reliability of such systems and circuits depends greatly on the reliability and accuracy of operation of the LSI devices and, thus, a need has arisen for new and sophisticated equipment and procedures for testing of these circuits. Such testing is relatively difficult because of the great number of different

functional sections in each device. The problem is further compounded by the limited number of test nodes available to each integrated circuit for the connection of input and output signals.

Most of the functional sections of the integrated circuits consist of either combinational logic circuits or sequential logic circuits or some combination thereof. A combinational logic circuit is defined as one that consists entirely of gates (AND, OR, etc.). In a combinational logic system, no clock is required, and after the inputs have been established (disregarding settling time), the output is immediately available for checking to determine whether it conforms to the output signal that the circuit should correctly produce in response to the specified input signal. On the other hand, sequential circuits require a sequence of changes in the input test signals, such as a clock, before an output signal, produced in response to the test signals, can be examined to determine if the device correctly responded. Because of the complexity of the digital circuits and the fact that there exists only a limited access to the integrated circuit chip's circuits via the IC pins, many different test signals must be generated before all of the functional capabilities of the LSI device can be checked. In a great many instances, an output signal must be checked as to the pattern of one's and zero's that is produced in response to a known set of input test signals to determine if the chip is working properly.

It is thus apparent that an apparatus for testing circuit assemblies containing LSI circuits must be able to develop and analyze a large quantity of data and test signals. Further, the test apparatus must be adapted to perform tests on a large number of different LSI circuits having widely different transfer functions. To best accomplish this requirement, a computer controlled test system is preferred. The versatility of test programs both to generate the necessary test signals and to analyze the resulting response signals make the computer a necessary element of a test system for digital circuits having LSI devices. Although the computer offers great flexibility in selecting tests to be performed, often the response signal produced by the generated test signals consists of bit streams of data that would require excessive computer storage and execution time to analyze each and every bit so produced. Therefore, a technique of compressing the bit stream down into something that can readily be assimilated by the computer to obtain maximum usage of the computer's capabilities would be desirable. This compression of the long bit streams can be accomplished by using a cyclic redundancy check (CRC) coding technique, which logically combines each bit with those that went before, to generate a compact digital code or signature. This signature represents, almost uniquely, the length and pattern of one's and zero's that occurred. The computer could then compare the measured code against a code for a correct response, to determine if the device is functioning properly.

A limitation of known computer-aided testers is the fact that the computer remains operatively tied into the test circuit during the performance of the test, because it is used as a source of test data. Because many LSI devices require lengthy and complex test signals in order to properly simmulate normal operations of the device, and because of speed limitations imposed by software-generated test signals, these types of computer-aided systems are capable of performing only a lim-

ited number of tests on these devices within a given time interval. However, if a computer-aided tester were provided which used intermediate test circuits to generate the test signals and to perform the functional tests, leaving for the computer only the initialization of the tester circuits prior to the test and the analysis of the results following the test, the power and flexibility of the computer could effectively be utilized.

Thus, it would be advantageous to provide a computer-controlled in-circuit digital tester for testing digital circuits employing the complex integrated circuits resulting from LSI technology in which appropriate test signals are generated and functional tests performed by intermediate test circuits, the results of which are analyzed by the computer.

SUMMARY OF THE INVENTION

In accordance with this invention, an automatic, computer-controlled digital in-circuit tester is provided for controlling a test cycle in which digital test signals are generated for a circuit under test. A response signal generated from that circuit in response to the test signals is checked for a proper response. A set of selectable electrical node test pins are provided, to contact the circuit interconnections of the circuit under test. These test pins permit the application of the test signals at selected points of the circuit and the monitoring of a response to those signals. The test signals are applied to the circuit under test through a set of selectable test signal switches associated with each of the test pins. Through processor control, a selected test pin has one switch from its associated set of test switches selected, to either apply a test signal to the test pin or to connect the test pin to a response signal bus. A digital test-signal generator is provided for each set of test switches to generate one signal from a set of selectable digital test signals. Among the set of digital test signals are signals which have the characteristic that identifies them as a Gray code.

A test controller, responsive to the processor, is provided for controlling the generation of a test cycle in which the digital test signals are generated. The response signal generated during the test cycle is monitored by a functional tester to perform intermediate processor selected tests. One of the functional tests is the determination of the signature of the response signal by generation of a cyclic redundancy check code. The result of the functional tests is inputted to the processor, where it is compared to the expected response to determine if the circuit under test has functioned properly.

BRIEF DESCRIPTION OF THE DRAWINGS

For a fuller understanding of the nature and objects of the invention, reference should be had to the following detailed description taken in connection with the accompanying drawings, in which:

FIG. **1** is a block diagram of the computer-controlled digital circuit tester;

FIG. **2** is a block diagram of the test signal generator;

FIG. **3** is the timing diagram for the set of selectable Gray code digital test signals;

FIG. **4** is the circuit diagram of the pin memory data transfer controller;

FIG. **5** is a circuit diagram of the test signal address generator and the D & E sync generator;

FIG. **6** is the circuit diagram of a test signal D switch driver;

FIGS. **7**(*a*) and **7**(*b*) are block diagrams of the test controller, the D, E, F & G switch selector and the functional tester;

FIG. **8** is a circuit diagram of the listen enable and start-of-test cycle generators;

FIG. **9** is a circuit diagram of the functional tester; and

FIG. **10** is a timing diagram which illustrates the generation of a listen enable signal.

Similar reference characters refer to similar parts throughout the several views of the drawings.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

It will be helpful in understanding the following discussion to define certain logic terms. Each of the logic signals to which reference is made in the following discussions will have one of two possible logic states, a logic 1 or a logic 0. A logic signal will be designated as a true signal without an asteric following the mnenomic. As an example, CLOCK would be a true signal while CLOCK* would be its inverse. Each logic signal, be it the true signal or its inverse, will have an asserted and unasserted state. In the case of CLOCK, a true signal, the asserted state will be a logic 1 and the unasserted state a logic 0. For CLOCK*, the reverse is true, the asserted state is logic 0 and the unasserted state is logic 1. A signal goes "true" when it switches from the unasserted to the asserted state and vice versa when it goes "false." Lastly, a flip-flop is in a logic 0 state when the Q output is at a logic 0 and the Q* is at a logic 1. In the logic 1 state the outputs of the flip-flop are in the reverse states.

Referring first to FIG. **1**, a block diagram of the computer controlled digital in-circuit tester is shown, with a central processing unit (CPU) **100** having a set of input/output (I/O) ports **102** that are used to communicate between the CPU **100** and the remaining circuits of the digital tester. I/O ports **102** contain standard interface circuits for interfacing the CPU **100** to a peripheral device. As used herein, the term "central processing unit" is meant to include all programmable or programmed devices of any size, such as microprocessors, minicomputers, computers, time-share computers, main frame computers, batch processors, data processors, etc.

The digital tester **101**, which responds to commands from the CPU **100**, is composed of test controller **104**, test signal generator **108**, functional tester **106**, board select decoder **114**, D, E, F & G switch selectors **116**, reed switches **120** and a bed of nails **122**. The bed of nails **122** consists of an array of selectable test pins that are contactable with the circuit interconnection nodes of the logic circuits on the printed circuit board of device under test (DUT) **124**. The DUT **124** is a printed circuit board assembly in which the interconnections between the various components are for the most part made with copper lands. Each DUT **124** will have its own preselected array of test pins that form the bed of nails **122** which contacts the interconnection points or electrical nodes of the circuits on the DUT. The test pins that will be used in testing the DUT **124** in each test cycle is selected from the bed of nails **122** and programmed into the processor. The DUT **124** is placed over the bed of nails **122** and a vacuum applied to cause the DUT PC board assembly to move down and contact the test pins in the bed of nails **122**. The board is caused to move a sufficient amount to cause the

spring loaded test pins to compress. This ensures that the test pins are contacting the interconnection nodes of the DUT **124** with sufficient force to penetrate the copper land.

Each pin in the bed of nails **122** has an associated set of selectable switches, designated as the D, E, F & G switches, connected to it. It should be noted here that the D, E and G switches are provided as a safety feature to protect the digital tester **101** internal circuits from excessive logic voltages that may appear on the electrical nodes of the DUT **124** by isolating each test pin through these switches.

For the digital tester **101** to work, the D, E and G switches do not have to be provided. However, the F switch is provided so that the test pin which will contact the output test signal node can be connected to the response line **128**. Therefore, the set of selectable switches associated with each test pin could be as few as one but as many as desired. As shown in FIG. **1**, one terminal of each of these selectable switches is connected to the test pin. During each test cycle, each of the selected test pins that contact the DUT **124** can either conduct an input test signal to the DUT or can conduct the selected output signal for the DUT, or it can alternately do both. If the selected test pin is to input an input test signal, the switch will be selected. The terminals of the E and G switches for each of the test pins that is not connected to its associated test pin are bussed together, respectively. The E switch selects the EXT CLOCK signal from the DUT to be applied to the master clock generator **706** (see FIG. **7**(*a*)). The F switch selects the node of the DUT that is to be the response signal and applies it to the functional tester **106** (see FIG. **7**(*a*)). Each test pin in the bed of nails **122** has the capability of applying a preselected digital test signal to DUT **124** through its D switch when the switch is selected. Each test pin has an associated digital test signal generator whose output can be connected to the test pin through a D switch.

If the test pin is to be connected to the electrical node that is the output signal for the circuit under test, switch F is selected. The F switches for each of the test pins in the bed of nails **122** are also bused together to form the response signal line **128**. Response signal line **128** is inputted to the functional tester **106**, where one of four functional tests is performed. Because of the large number of test pins available in the bed of nails **122** (for the preferred embodiment 1,024 pins), practical considerations of constructing the tester require that the test pins be grouped into smaller subsets on boards to accommodate the circuits required to contain the D, E, F & G switches, to select the appropriate ones of those switches for each test pin used in the test, and to generate the digital test signals for the test. These circuits are chosen for inclusion in the subsets because they are duplicated for each test pin in the bed of nails **122**.

For the preferred embodiment, the bed of nails **122** is divided into groups of sixteen test pins. Within each group, the E, F and G switches are bussed together. Further, the bussed E, F and G selectable switches are connected to buses between the groups of sixteen test pins through selectable switches KFD, KED, and KGD. These selectable switches, KFC, KED and KGD, provide isolation for the internal bussing of the sixteen test pins from the external bussing between the groups of switches. But, in any event, each E, F and G switch for each test pin is connectable to the same bus.

The circuits required to generate sixteen separate digital test signals for each of the sixteen test pins in the subset, to select which of the four selectable switches for each test pin that is to be used during the test cycle, and to contain the actual reed switches and their coil drivers to provide the D, E, F and G contacts, are mounted on a single PC board assembly. Thus, for the preferred embodiment, a total of **64** boards are required for a bed of nails of **1**,024 test pins. As shown in FIG. **1**, each PC board assembly **103** containing the above described circuits is composed of a pin memory **112**, test signal drivers **118**, a board select decoder **114**, D, E, F & G switch selectors **116**, and reed switches **120**.

Still referring to FIG. **1**, the digital tester is used as follows: A circuit diagram of the device to be tested is examined to identify the circuits or chips that are to be tested. In general, all nodes will be contacted by a test pin, even unused elements of the integrated circuits. The electrical nodes that are to be used in a test cycle as either an input node or as the circuit under test response node are identified and assigned the number that corresponds to the test pin number that will contact that node when the board assembly is placed on the bed of nails. Knowing how the circuit under test is intended to work, computer routines are generated that will, when executed by the computer, cause the tester to generate appropriate test signals to the electrical nodes of the circuit under test. The tester **101** circuits will monitor the response signal and perform intermediate tests on the signal. Under computer control, the tester **101** will transmit the results of the intermediate tests to the computer, where a comparison between the measured response and the expected response determines if the circuit has functioned properly.

Each integrated circuit in the circuit under test is tested during a test cycle defined to be that period during which the digital test signals are actually being applied to the circuit under test. Although all of the test parameters are specified by computer software, the actual tests are carried out, for the most part, independently of control of the computer. That is, the computer specifies the type of test that is to be performed, the length of the test cycle, the types of test signals that are to be generated, the test pins to be selected, etc., prior to initiation of the test cycle. Once the test cycle is initiated, the CPU **100** must wait until the test cycle is finished before it acquires the results of the intermediate tests. As a result, the CPU supplies the digital tester **101** with the initial conditions for the test to be performed, before it causes the test cycle to begin.

The CPU **100**, acting through I/O ports **102**, initialize the circuits of tester **101** prior to a test cycle, by sequentially addressing each test pin that is to be used in testing of the circuit under test, and selects and latches at least one of the D, E, F or G switches for each of those selected test pins. Where appropriate, the KFD, KED and KGD switches are also selected and latched. Having selected and closed a switch for each test pin that will apply a test signal to an input node of the circuit under test, and having selected and closed the F switch of the test pin that will be the response signal, the CPU **100** next sequentially transfers to the pin memories **112** the data necessary for the digital test signal generators to generate the appropriate selected test signal for the selected nodes of the circuit under test. Pin memory address and data load generator **110**, in response to commands and data from the cPU **100**, stores digital data in pin memory **112**. This data, when read during

the test cycle, generates a pattern of one's and zero's on the input of test signal drivers **118**. In response to the pattern, the drivers **118** generate the digital test signals that are applied to the selected test pins through their closed D switches.

To complete the initialization of the tester **101**, the CPU **100** strobes into test controller **104** the parameters which specify: (1) Whether an internal or an external clock reference signal is to be used to generate the digital tester **101** system clock; (2) data which determines the frequency of the system clock derived from the selected reference clock; (3) which of the intermediate tests is to be performed on the response signal; (4) the length of the test cycle that is to be performed; (5) the time during the test cycle in which the response is tested and the time during which the response is ignored; and (6) data to generate a threshold voltage which enables the digital circuit tester to interface to a wide range of logic voltage levels from different DUT's.

Having initialized the circuits of tester **101**, the CPU **100** may now initiate a test cycle by issuing the appropriate command to the test controller **104**. At the completion of the test cycle, the CPU **100** transmits a command to the tester **101** to transfer the contents of the functional tester to the computer. A comparison is then made between the actual result that would have been produced from a properly functioning circuit, to determine if the circuit is working. The preceding discussion has been given to explain how the tester is used, so that the following detailed description of the circuits which implement the above-described functions may more readily be understood.

Shown in FIG. 7(*b*) are board select decoder **114**, D, E, F & G switch selectors **116** and reed switches **120**, which function to select and close one or more of the four selectable reed switches for the test pins used during the test cycle. Board select decoder **114** and D, E, F & G switch selectors **116** function as the switch-selecting means for selecting which reed switch is to be closed during the test cycle. A 8-input NAND gate **728** decodes the board address signals, BA0 through BA6 and their inverse, to generate the board select signal BS if this board is selected.

Each slot of the digital tester into which a board is to be plugged has a unique address assigned to it. As previously discussed, each board contains the circuits for sixteen test pins. This board address is encoded into the connector wiring for the slot, such that the appropriate board address signal (BA0 through BA6 or its inverse) is applied as one input to NAND gate **728**. The output of NAND gate **728** is OR'ed in NOR gate **730** with a board address override signal (BAOR)* to generate the signal BS. The signal BAOR* is generated when a board select signal is to be generated on all of the boards simultaneously. The board address signals are generated by the test controller **104** in response to commands and data from CPU **100**. CPU **100** also generates reed addresses (RA0 through RA3) and reed group addresses (RG0* and RG1*) which D, E, F and G switch selectors **116** decode, to select, for each of the sixteen test pins on the addressed board, one of the four selectable switches.

Reed addresses RA0 through RA3 and reed group addresses RG0* and RG1* are inputted to D, E, F and G switch selectors **116** to address a plurality of latches, to both store and reset the selection of the selectable switches. The RG0* and RG1* signals are decoded to select one of the four selectable switches (D, E, F or G), and the address signals RA0 through RA3 are decoded to select one of the sixteen test pins on a board. Since the selection process for the D, E, F & G reed switches is the same, only an explanation for the selection of the D switches will be given.

Still referring to FIG. 7(*b*), in the clearing process for the D reed latches **732** and **734**, a BS signal, when true, enables clear reed switch decoder **738**, so that the reed group addresses, on the occurrence of RCLR* from CPU **100**, generate one of four possible reed switch clear signals: CD*, CE*, CF*, or CG*. For clearing of the D reed latches **732** and **734**, the signal CD* is generated. This signal is applied to the clear input of the latches **732** and **734** to clear any latches that were set from the previous test cycle.

In the reed switch selection process, reed addresses RA0 through RA2 provide a three bit octal address for latches **732** and **734**. Reed address RA3, in conjunction with the reed group signals RG0 and RG1, are decoded by set reed switch decoder **736**, on the occurrence of R STROBE*, to generate four pairs of enabling signals, ED0* and ED1* through EG0* and EG1*, with each pair selecting the pair of reed latches for each of the four selectable switches for each test pin. In other words, for the D switches, enabling signals ED0* and ED1* are generated to enable reed latches **732** and **734**, respectively. With the set/clear* (S/C*) signal at a logic one, the individual latch addressed by the reed addresses RA0 through RA2, in conjunction with the enable signal from set reed switch decoder **736**, loads a selection command into the addressed latch. The outputs from D reed latches **732** and **734** are applied to relay drivers **742** to energize the selected D reed switch. In this manner, each of the selectable switches associated with each of the test pins may be selected and latched closed prior to the start of the test cycle.

Again referring to FIG. **1**, test signal generator **108** is shown, composed of pin memory address and data load generator **110**, pin memory **112** and test signal drivers **118**. Identical pin memory **112** and test signal driver **118** circuits are contained on each of the tester boards in the digital tester **101**. The output from pin memory address and data load generator **110** is bussed to each of the pin memory **112** and test signal drivers **118** contained on each of the system tester boards. Pin memory **112** responds to the board select signal BS to enable the data on the bus from pin memory address and data load generator **110** to be inputted to the selected board. In this way, the circuits for pin memory address and data load generator **110** do not have to be duplicated for each board in the tester in order to generate a digital test signal for each test pin. The function of the test signal generator **108** is to generate, during the test cycle, one of the digital test signals from the set of selectable test signals that includes the Gray code set of signals. Since the operations of pin memory address and data load generator **110**, pin memory **112** and test signal drivers **118** are identical for each of the tester boards, only a discussion of one will be given.

Referring now to FIG. 2(*a*) and 2(*b*), which illustrates a typical test signal generator **108**, pin memory address and data load generator **110** is shown, composed of pin memory data transfer controller **200** test signal address generator **202**, D and E sync generator **204**, and pin memory address multiplexer **206**. The function of the pin memory address and data load generator **110** is to generate memory addresses and memory data for pin memory **112**. Pin memory addresses are generated at

two different times. First, prior to a test cycle, data must be transferred and stored in pin memory **112** that will generate the digital test signal to be applied through the selected D switches for each of the selected test pins to the circuit under test. Second, during the test cycle, addresses must be generated to pin memory **112** to read the contents of the memory to generate the desired test signal.

The pin memory address and data input signals which program the pin memories **112** prior to a test cycle are generated by the pin memory data transfer controller **200**. Pin memory data transfer controller **200**, responding to inputs from CPU **100**, generates an 8-bit data word on memory data lines MD0 through MD7. These data lines are inputted to pin memory **112** where tri-state buffers **210**, enabled by the BS signal for this board, pass the data to the input of the memories **214**. At the same time, pin memory data transfer controller **200** generates a set of data transfer memory addresses, DTMA0 through DTMA3, which are inputted to pin memory address multiplexer **206**. Additionally, pin memory data transfer controller **200** generates two control signals, write enable MW*, and data transfer memory address mux, DTMA MUX. The signal DTMA MUX is inputted to pin memory address multiplexer **206** to cause the data transfer memory address lines to be multiplexed onto the memory address lines MA0* through MA3*, which form the input address lines for the memories **214**. The control signal MW* is inputted to the pin memory write enable decoder **208**, to enable a write cycle to the memories **214**. Also inputted to pin memory write enable decoder **208** are the memory group addresses MG0* and MG1*. The two addresses are inputted directly to decoder **208** from the CPU **100** through I/O ports **102** to generate WE0* through WE3* in the pin memory write enable decoder **208**.

Each of the memories **214** is able to generate digital test signals for two of the D selectable switches. Thus, for a total of sixteen selectable D switches per board, **8** memories are required. The devices that are used in the preferred embodiment of the invention for the pin memories are 16×4 bit random access memories such as a 74LS189 manufactured by National Semiconductor, Inc. It will be appreciated by those of ordinary skill in the art that memory devices of different storage capacity could be substituted for the memories used in the preferred embodiment, such as four 16×1 memory chips. Therefore, each pin memory requires four bits of data input and four bits of address input to address and store data in each of the addressable memory locations.

Since the data lines from pin memory data transfer controller **200** total **8**, two memories or two test signal generators are programmed at the same time. Therefore, by bussing a write enable signal to two consecutive pin memories, only four pin memory write enable signals need be generated. The function of pin memory write enable decoder **208** is to generate those four write enable signals. The memory group address lines MG0 and MG1 specify which of the four groups of two-pin memory chips are to be enabled, and when MW* is true, decoder **208** generates one of the four pin memory enable signals WE0* through WE3* specified by MG0 and MG1.

Test signal address generator **202**, responding to a START CYCLE* from test controller **104**, generates the Gray code memory address lines, GMA0 through GMA3, which are also inputted to pin memory address multiplexer **206**. These address signals are generated during a test cycle to address and output the contents of the memories **214**, to generate the test signal which the D selectable switches will apply to the circuit under test. The Gray code memory addresses are multiplexed on to the memory address lines MA0* through MA3* by pin memory address multiplexer **206**, when the system DCLR* signal and the control signal from pin memory data transfer controller **200**, DTMA MUX, are both unasserted. A third mode of addressing the pin memories is also possible. This occurs when both the control signal DTMA MUX and DCLR* are at a logic **0**. For this condition, CPU **100** delivers the memory address lines directly from one of the I/O ports **102** to pin memory address multiplexer **206**. That address then appears on the memory address lines MA0* through MA3*.

When a test cycle begins and Gray code memory addresses are generated by test signal address generator **202**, D sync and E sync generator **204**, in response to these addresses, generates the synchronization signals DSYNC* and ESYNC*. These two synchronization signals are used by the test signal drivers **118** in the generation of the digital test signals that are applied to the DUT via the D selectable switches.

Referring now to FIG. **4**, which shows the circuit diagram for pin memory data transfer controller **200**, system commands CMD2* and CMD3*, generated in test controller **104**, are used to select one of two operating modes for the controller **200**. In the first mode, data transfer controller **200** can pass the 8-bits presented by CPU **100** via I/O ports **102** to the memory data lines MD0 through MD7; or, in the second mode, controller **200** may accumulate sixteen consecutive 8 bit data values from the CPU before that data is placed on the memory data lines. To operate in the first mode, system command CMD14* is asserted. This signal is inputted to NOR gate **430**, whose output is inverted by gate **432** to generate MW* which, as previously discussed, enables pin memory write enable decoder **208** (see FIGS. 2(*a*) and 2(*b*)) to write the 8 bits into the memories **214**. With the assertion of CMD14*, the data that is presented by CPU **100** to the "A" inputs of multiplexer **424** is muxed onto the memory data lines and strobed into the pin memories **214** enabled by one of the four write enable signals, WE0* through WE3*, generated on the output of pin memory write enable decoder **208**.

For the first mode of operation, the output of pin memory address multiplexer **206**, MA0* through MA3*, is derived from an address specified by CPU **100** on the data lines of one of the output ports of I/O ports **102**. The signal DTMA MUX is not asserted in this mode, but the signal DCLR* is. Therefore, pin memory address multiplexer **206** is selecting the data lines from one of the I/O ports **102** output ports to generate the memory address lines. For each 8 bit data word that is to be strobed into the pin memories, a CMD14* signal must be asserted.

For the second mode of operation of data transfer controller **200**, in which sixteen consecutive 8 bit data words will be stored before transferring to the memories **214**, two steps must occur. First, each 8 bit data word must be strobed into an 8 bit shift register **400**, and second, the contents of shift register **400** must be transferred into 16×8 bit shift register **422**, which is acting as the buffer storage device. When shift register **422** is full, system command CMD2* is asserted to initiate the sequence of transferring the contents of shift register

422 through multiplexer 424 onto the memory data lines. For each 8-bit data word that is supplied from I/O ports 102 output port number 3 to the input of shift register 400, PORT 3 STROBE* is asserted to strobe the 8-bit data word into the shift register 400. At the same time, PORT 3 STROBE* resets set-reset flip-flop 402 to a logic zero. The Q output from flip-flop 402 is inputted to NOR gate 404, whose output switches to a logic zero and removes a clear signal to cascaded binary counters 410 and 412. Removing the clear signal to these two counters enables them to begin counting a 2 MHZ internal clock generated by test controller 104. The Q_C and Q_D outputs from counter 410 and the Q_A output from counter 412 are decoded in OR gates 416 and 418 to provide an enabling signal when any one of these three signals is true. This enable signal is inputted as one input to AND gate 420. The other input of AND gate 420 is the Q_B of counter 410, which is the highest frequency signal on the Q outputs of counters 410 and 412 that are used by controllers 200. As a result, the output of gate 420 generates 7 shift pulses to shift register 400 when the enable signal on the output of OR gate 418 is at a logic 1. Inverter 414 inverts the Q_B of counter 410 to generate 8 shift pulses to shift register 422. Because shift register 400 is presenting one of the 8 data bits to the input of shift register 422 before the generation of any shift pulses, only 7 shift pulses are required by register 400 to input all 8 bits to register 422; while 8 pulses are required by register 422 to load that data.

When the output of NOR gate 404 removes the clear signal to the binary counters 410 and 412, they begin to generate output signals each of which is half the frequency of the previous output signal. Thus, selecting three successive outputs would generate 8 possible states, selecting 4 successive outputs would generate 16 possible states, etc. Using this technique, the Q_B output of counter 410 generates 8 cycles from the time the enable signal from gate 418 went true until the Q_B output of counter 412 goes true. In this manner, the 8 bit data word that was strobed into shift register 400 by PORT 3 STROBE* is serially clocked into shift register 422. When the Q_B output of counter 412 goes true at the end of the eighth shift pulse to shift register 422, set-reset flip-flop 402 is set to a logic one. This causes NOR gate 404 to once again assert a clear pulse clearing counters 410 and 412 back to a counter of 0. Thus, in the second mode, the above-described sequence is repeated for sixteen consecutive 8 bit data words.

When shift register 422 contains sixteen 8 bit data words, asserting CMD 9* initiates the transfer of the contents of shift register 422 to the memories 214 (see FIGS. 2(*a*) and 2(*b*)). With the assertion of CMD 9*, set-reset flip-flop 401 is cleared to a logic zero. This causes NOR gate 404 to remove the clear signal to the binary counters 410 and 412. Also, the Q output of flip-flop 401 causes the 8 bit multiplexer 424 to select the output from shift register 422 applied to its "B" inputs, as the source of the data for the memory data lines MD0 through MD7. Inverter 426 inverts the select line of multiplexer 424 to generate the control signal DTMA MUX that is used by the pin memory address multiplexer 206 (see FIG. 2(*a*)) to enable the data transfer memory address lines DTMA0 through DTMA3, generated by counters 410 and 412, to be multiplexed onto the memory address lines MA0* through MA3*. The signal DTMA MUX is ANDED with the Q_B output of counter 410 by NAND gate 428 to generate MW* on the output of inverter gate 432. Thus, a write enable clock is generated for each memory address specified by the data transfer addresses DTMA0 through DTMA3 to store in the memories 214 the 8 data bits multiplexed onto the memory data lines MD0 through MD7 from shift register 422.

The above sequence continues until sixteen 8 bit data words from shift register 422 have been transferred to the pin memories. At the completion of the transfer, the Q_C of counter 412 goes true causing interter gate 408 to set flip-flop 401 to a logic 1. This causes NOR gate 404 to once again assert a clear signal to the counters 410 and 412. Because the Q_C output of counter 412 initiates the clear signal, the Q_B output of counter 410 will generate 16 cycles before the counting is stopped. Thus, when Q_C goes true and initiates the clear to counter 410 and 414, the sequence of transferring the sixteen 8-bit data words to the memories 214 is complete.

Referring now to FIG. 2(*b*), which is a block diagram of pin memory 112 and pin drivers 118, the contents of memory 214 used to generate one of the Gray code test signals are shown as a sequence of ones and zeros stored in the sixteen memory locations. Shown above each of the bit memory locations is the pin memory address, in hexa-decimal notation, that will produce on the memory output data and enable lines, D0 and E0, the bit contained in the memory locations shown below the address.

The generation of a digital test signal which are applied to the contacts of the selectable D switches from data contained in the contents of memory 214 are the same, and only a discussion of one will be given. Still referring to FIG. 2(*b*), the sequence of ones and zeros produced on the output by the addressing of memory 214 during a test cycle is inputted to the DR0 switch driver 216. The output signal from this driver is the digital test signal that drives the DUT via the selectable DR0 switch. The character of the digital test signal that is generated from the data stored in memory 214 is controlled by the sequence of addresses with which the memory 214 is addressed. Two memory 214 output signals are required to generate a digital test signal, one called the data bit; the other the enable bit. The data bit is the output signal from memory 214 that is lbeled D0, while the enable bit is the output labeled E0. As will more fully be discussed below, each memory location, from memory address 1 through E, can select a different wave form from the set of Gray code wave forms to be generated by the DR0 switch driver 216.

Turning now to FIG. 3 and still referring to FIG. 2(*b*), the test signal timing diagram is illustrated for various selectable Gray code test signals, each signal including an initialization and preset portion. There are sixteen addressable memory locations in memory 214. The contents of the memory 214 for addresses 0 and F control the initialization and preset portion of the digital wave form. The initialization and preset portion of the digital wave form is generated at the start of a test cycle. With two of the memory 214 storage locations used up for the initialization and preset data, only fourteen Gray Code test signals can be specified by the remaining memory locations. This number, of course, can be increased or decreased by increasing or decreasing the memory capacity of memory 214. It is the distinguishing characteristic of a Gray code set of wave forms that, when all the waveforms are viewed simultaneously, for any given cycle of a clocking wave form which generates the digital signals, only one signal will have a transition from one logic level to the other. In other words,

no more than one transition in all the wave forms that comprise the Gray code occur for any given clock cycle. To select one of the Gray code test signals, a "1" is recorded in pin memory 214 at the address that corresponds to the desired wave form, and zeros are recorded at the other addresses. Thus, for wave form number 2, a 1 is recorded in memory location 2; or for wave form number 13, a "1" is recorded in memory location D.

In addition to the fourteen Gray Code test signals that can be generated from data stored in memories 214, other digital test signals are possible, such as logic high, logic low, preset high (a single positive pulse at the start of the test cycle), preset low (a single negtive pulse at the start of the test cycle) and the many permutations that are possible in the basic Gray Code signals that are generated by the use of the initialization and preset data a long with the enable data recorded in the enable portion of memory 214. An example of just such a permutation is illustrated in FIG. 3 as signal f_2. The following is a discussion of how the data in memory 214 generates the digital test signals.

Shown in FIG. 3 is a portion of the sequence of pin memory addresses that are generated during a test cycle. Also illustrated in FIG. 3 are the digital test signals that are generated on the output of DR0 switch driver 216, according to the data on the D0 and E0 output lines of the pin memory 214. A transition in the output digital test signal from DR0 switch driver 216 is permitted each time that a 1 is outputted on the D0, line provided that the E0 line has previously or is concurrently outputting a one. Referring to FIG. 3, the four waveforms f_1, f_1*, preset high f_1, preset low f_1* are shown. Disregarding the initialization and preset portion of those waveforms, it can be seen that on each occurrance of memory address 1, a transition in f_1 occurs. As will be discussed below, the DRIVE ENABLE f_1 signal can modify the illustrated waveforms for f_1; but for the f_1 waveforms shown in FIG. 3, DRIVE ENABLE f_1 went true during the initialization portion of the test cycle.

For the initialization and preset time of the test cycle, the sequence of pin memory addresses is, in sequence, address 0, address F, an address designated as "don't care", and once again, address F. The address designated as "don't care" is so labeled because regardless of what address is generated by test signal address generator 202, signals DSYNC and ESYNC are absent, as nothing is permitted to happen in the DR0 switch driver 216 to cause a change in the generated test signal. Illustrated in FIG. 3 for the wave forms f_1 and its derivatives showing the four possibilities for the initialization and preset portion. The generation of these four wave forms is possible for each of the fourteen Gray Code test signal. For the wave forms illustrated, the signal DRIVE ENABLE f_1 was asserted at address 0 in the initialization and preset portion of the test cycle by having a "1" recorded in the enable portion of memory 214 at address 0. A different result would have occurred had the enable bit been stored in a different memory location. This result is illustrated for the wave form f_2 in which the enable portion of memory 214 has a "1" recorded in location 3 and location 4. The result of two 1's recorded in the enable portion of the memory 214 is an enabling of the DR0 switch driver 216 on the first occurrence of a "1" on the E0, and a disabling of f_2 on the second occurrence of a "1" on E0.

The illustrated wave form f_2 in FIG. 3 is the signal generated from the data that is shown as stored in memory 214 in FIG. 2(*b*). On the first occurrence of the memory address 3, DRIVE ENABLE f_2 is asserted and on the first occurrence of address 4, DRIVE ENABLE f_2 is cleared. The dotted wave forms that are shown for the signals f_2 and DRIVE ENABLE f_2 are the signals that would have been generated had there only been a "1" stored in the enable bit address location 0. As illustrated in FIG. 3, a transition in the DRIVE ENABLE f signals occur on the first occurrence of a pin memory address with a "1" stored in the enable portion of memory 214 for that address rather than on every occurrence of that address. This is because the illustrated clocking signal (ESYNC) in FIG. 3 which clocks the transitions in the enabling flip-flop 602 (see FIG. 6 and the discussion below) has been selected to occur only on the first occurrence of a pin memory address. A more detailed discussion of the possible variations in the generation of the clocking signal ESYNC is given in the discussions of the D sync and E sync generator 204.

Still referring to FIG. 3, refer also to FIG. 5 which is the circuit diagram of the test signal address generator 202 that generates the sequence of pin memory addresses as illustrated in FIG. 3. With the assertion of START CYCLE*, shift register 500 is loaded with a bit pattern that produces on the Q_A through Q_D outputs, 0101, respectively. For four consecutive cycles of the system clock MCKL*, the signals INIT*, CLOAD*, and PRESET* are generated. These three wave forms are shown in FIG. 3. The signal CLOAD* loads a fourteen bit binary down counter 506 with an all 1's pattern. Counter 506 is formed from the cascaded connection of four four bit binary down counters (not illustrated). The output of counter 506 is inputted to the three-bit cascaded priority encoders 508 and 510 along with the signals INIT* and PRESET*. The outputs from encoders 508 and 510 are logically combined in NOR GATES 512, 514, 516 and inverter 518 to generate the Gray code memory address signals GMA0 through GMA3, which are inputted to pin memory 206 (see FIG. 2(*a*)). Down counter 506 counts down from an all 1's or maximum count to a count of 0. When counter 506 reaches a count of 0, one complete cycle of the Gray code test signals is complete. If more than one cycle of the Gray code signals are desired, the signal DCLR* from test controller 104 is not asserted, and down counter 506 continues to count down from a count of 0 to the next count which is once again an all 1's count to begin the next cycle. However, for this and each subsequent cycle in the Gray code signals, no initialization or preset addresses, 0 or F, will occur.

Two clocking signals are generated by the D and E sync generator 204 to be used by the test signal drivers 118 to generate the digital test signals on the output of the D switch drivers 216. These two signals are called DSYNC* and ESYNC*. FIG. 3 also illustrates these two signals. Except for the address "don't care" in the initilization and preset portion of the sequence of pin memory addresses and on the last occurrence of the "F" address in the test cycle, the signal DSYNC* is the same as the clock signal MCKL*. On the other hand, the signal ESYNC* has the characteristic that it may occur on the first occurrence of each of the pin memory addresses or may occur on the occurrence of any one or all of the memory addresses.

Referring still to FIG. 5, in which is shown the circuit diagram for the D and E sync generator 204, the signal

DSYNC* is derived from MCKL but is enabled only during a test cycle through AND gate **528** and inverter **530** by the signal DCLR*. Also, during the initialization and preset time of the test cycle when the third pin memory address is generated ("don't care" address), all input signals to priority encoders **508** and **510** are at a logic one. This causes the PRESET DISABLE output from priority encoder **510** to be at a logic 0. This level causes DSYNC* to remain high for that "don't care" pin memory address in the initialization and preset portion. Because changes in the output of the digital test signal from the D switch driver **216** are clocked when the signal DSYNC* goes false in the middle of a pin memory address, for the "don't care" pin memory address of the initialization and preset time, no transition in DSYNC* occurs; thus the label "don't care".

Still referring to FIG. **5**, the signal ESYNC* may be selected to occur on only the first occurrence of each of the pin memory addresses, or it can be selected to occur on every occurrence of any address or on every address. This flexibility is achieved as follows: A four-bit data word is inputted to the D sync and E sync generator **204** from the CPU **100** and on the assertion of CMD13*, is strobed into a sixteen-bit latch formed from addressable latches **532** and **534**. Each of the sixteen latches corresponds to one address in the possible sixteen pin memory addresses. The output from latches **532** and **534** are inputted to multiplexers **536** and **538**, respectively. Also inputted to multiplexers **536** and **538** are the Gray Code pin memory addresses GMA0 through GMA3. The multiplexed output from multiplexers **536** and **538** are bussed together to form an enabling signal to one input of AND gate **540**. The latches **532** and **534** can be programmed to contain all zero's or all one's or any of the combinations of one's and zero's that are possible. In operation, during the test cycle as the Gray Code pin memory addresses are generated, the contents of the latch from latches **532** and **534** that corresponds to the generated address is multiplexed to AND gate **540**. If a one was stored in the latch, AND gate **540** is enabled to pass one cycle of MCKL to OR gate **542** whose output, acting through inventor **544**, generates the signal ESYNC*. If a zero was stored in the latch, AND gate **540** is disabled and no ESYNC* signal will be generated. Thus, the signal ESYNC* can be programmed to occur on any address by storing a one in the appropriate latch in latches **532** and **534**.

It is also possible to have ESYNC* occur only on the first occurrence of the pin memory address during the test cycle. This is accomplished by a four-bit binary counter **522** in association with a four-bit magnitude comparator **520**. At the start of the test cycle, counter **522** is cleared to a count of **0**. The binary count from counter **522** is compared to the binary code on the Gray Code pin memory address lines GMA0 through GMA3, by four-bit magnitude comparator **520**. When there is a count match, AND gate **524** is enabled by the "A=B" output of comparator **520**, to permit one cycle of MCKL to be applied as the other input to OR gate **542** and thus to generate the signal ESYNC*. The output from AND gate **524** is inverted by inverter **526** and provides a clock signal to counter **522**. This increments counter **522** to the next address. The first occurrence of this address by the pin memory address generator **202** will enable another ESYNC* to be generated. Once counter **522** has been incremented sixteen times and reaches a count of **0** there will never be another match in magnitude comparator **520**, because the Gray Code memory address is an all 0's or "0" address only during the initialization and present time, which occurs only at the start of the test cycle.

The signals DSYNC* and ESYNC* are inputted to test signal drivers **118** to clock each DR switch driver **216** to generate the digital test signal on the output of the driver (see FIG. **2**(*b*)). Shown in FIG. **6** is a circuit diagram of a typical DR switch driver **216**. Since all of the DR switch drivers **216** of test signal drivers **118** are identical in operation, only a discussion of one will be given. The data (D0) and enable (E0) lines from memory **214** for test pin **1** of the bed of nails **122** are inputted to D switch driver **216** of FIG. **6** to provide the J and K inputs for flip-flops **600** and **602**, respectively. Flip-flop **600** is clocked by DSYNC which is the buffered inverse of DSYNC* (see FIG. **2**(*b*)), while flip-flop **602** is clocked by ESYNC, also buffered. The Q and Q* outputs from flip-flop **600** provide inverse digital signals that control the conduction state of a complimentary pair of field effect transistors Q_1 and Q_2. These two transistors switch the output signal DR0 between the power supply and ground potential for the DUT being tested to provide the voltage swing for the digital test signal. Ground potential for the DUT is the same as for the tester.

Before the Q and Q* outputs of flip-flop **600** are allowed to control the transistors Q_1 and Q_2, the enable flip-flop **602** must be clocked to a logic **1** by ESYNC. Open-collector NAND gate **604** combines the Q output of flip-flop **602** with the Q output of flip-flop **600** to provide the control signal for transistor Q_1. Open-collector AND gate **612** combines the Q output of flip-flop **602** and the Q* output of flip-flop **600** to provide the control signal for transistor Q_2.

Driver output DR0 has three allowable states: First, when neither transistor **Q1** nor transistor **Q2** is conducting, the driver DR0 is said to be disabled. When the driver is disabled, it does not stimulate the device under test. This disabled state is obtained whenever enable flip-flop **602** is cleared to a logic zero. The output of AND gate **612** is low, turning off N-channel-transistor **Q2**. The output of open-collector NAND gate **604** is pulled up to "Driver V+" potential by resistor **608**, turning off P-channel transistor **Q1**. In the disabled state, the output of the driver will be an open circuit. Therefore, it is possible to have both the D and the F switch for this test pin selected. During the test cycle, when the driver is disabled, the same node into which a digital test signal was or could have been inputted, a response signal could also be monitored. For some logic devices, that is the manner in which they function. For example, some memory devices require that an address be inputted on the same line that the contents of the memory specified by that address is outputted on. Because of the disable node of operation of the driver **216**, the D switches is not required in the set of selectable switches associated with each test pin in the bed of nails **122**. Second, when transistor **Q1** is conducting, the driver output will be high. This state is obtained whichever enable flip-flop **602** and data flip-flop **600** are both set. The output of open-collector NAND gate **604** is low, stimulating the P-channel transistor **Q1**. Third, when transistor **Q2** is conducting, the driver output will be low. This occurs when enable flip-flop **602** is set and data flip-flop **600** is cleared. The output of AND gate **612** is high, stimulating the N-channel transistor **Q2**. Note that for either transistor to conduct, the enable

flip-flop 602 must be set, and that transistors Q1 and Q2 may not conduct simultaneously. In addition, the transistors are able to pass 150 milliamperes, enough to drive a logic node "in-circuit".

Referring now to FIG. 7(*a*), which illustrates a block diagram of test controller **104** and functional tester **106**, the command decoder **710** of test controller **104** is shown connected to one of the CPU **100** I/O **102** ports. The function of command decoder **710** is to accept an 8-bit digital code from CPU **100** and decode it to generate one of thirty-two system commands CMD0* through CMD31*. Command decoder **710** also generates the miscellaneous system commands, such as board address override BAOR*, functional test COUNT*, functional test HIGH*, and EXT CLOCK SELECT*. Shown in Table 1 is a list of the system commands along with its functional name. System commands CMD5* through CMD7* are used to strobe date from the CPU **100** into latches (not shown) that function to generate other signals used by the tester **101** to perform various functions. The signals generated by these three system commands, CMD5* through CMD7*, are also shown in Table 1. In particular, the miscellaneous system commands mentioned above are generated by CMD7* (mode latch #2) in association with the data on the data lines illustrated in Table 1. The system commands that are generated by command decoder **710** are used to start and stop various functions within the digital tester **101**.

TABLE I

COMMAND	SKIP CONTROLLER COMMANDS	
CMD0*	Master Reset	
CMD1*	Trigger An Execution Cycle	
CMD2*	Reed Set	
CMD3*	Reed Clear	
CMD4*	Reed Group Clear (RCLR*)	
CMD5*	Control Reed Latch	Data Line Control Reeds
		0 Response Line Connect
		1 Connect E Pole Reed
		2 Ground E
		3 Stimuli F
		4 Ground G
		5 not assigned
CMD6*	Mode Latch #1	Data Line Mode Latch #1
		0 DUT − Reed
		1 DUT + Reed
		2 DUT + 5V Supply Relay
		3 DUT + RV Supply Relay
		4 not assigned
		5 not assigned
CMD7*	Mode Latch #2	Data Line Mode Latch #2
		0 Count*/High* Reg Select
		1 BAOR*
		2 EXT CLOCK SELECT*
		3 not assigned
		4 not assigned
		5 not assigned
CMD8*	Shift Result Registers	
CMD9*	Program Data Transfer	
CMD10*	MG & RA & RG Latch	
CMD11*	Threshold Voltage Latch	
CMD12*	Clock Division Latch	
CMD13*	ESYNC Set	
CMD14*	MEM Write	
CMD15*	Clear ESYNC Memory	
CMD16*	Not Assigned	
CMD17*	Not Assigned	
CMD18*	PICA Busy Set	
CMD19*	PICA Busy Reset	
CMD20*	Interupt Enable	
CMD21*	Interupt Disable	
CMD22*	X Relay Strobe ($\overline{\text{STROBE}}$)	
CMD23*	X Relay Master Clear (MCLR)	
CMD24*	Not Assigned	
CMD25*	Not Assigned	
CMD26*	Not Assigned	
CMD27*	Not Assigned	
CMD28*	Not Assigned	
CMD29*	Not Assigned	
CMD30*	Not Assigned	
CMD31*	Not Assigned	

In order to accommodate the various logic voltage levels used by different DUT's, test controller **104**, in response to input data from CPU **100**, generates a negative threshold voltage, (−) THRESHOLD, of a value somewhere between the logic low and logic high for that family of integrated circuits. This threshold voltage is summed with signals from the DUT to generate a voltage that is applied as an input to a comparator. When the DUT signal is equal to a positive threshold voltage, the summed voltage will be zero. A more detailed discussion of the summing circuits will be given below in the discussion of the response line interface **720**. The signal (−) THRESHOLD is generated when system command CMD18* strobes an 8-bit digital word from the CPU **100** into threshold voltage latch **700**. The output of latch **700** is inputted to digital-to-analog con-

verter 702, which generates a negative voltage specified by the binary contents of the threshold latch 700.

The system clock which is generated by and used in the digital tester 101 circuits as the master clock is generated by master clock generator 706. The system clocks MCKL and MCKL* are outputted by master clock generator 706 by dividing down an 8 MHZ oscillator clock signal from internal oscillator 708 in a divide-by-N counter. The value of N is specified by the contents of divide-by-N counter latch 704. System command CMD12* strobes an 8-bit data word (N) from CPU 100 into latch 704 to program the divide-by-N counter. Oscillator 708 also provides a 2 MHZ oscillator clock signal for use by the pin memory data transfer controller 200 (see FIG. 4). When an external clock other than the 8 MHZ internal clock is to be used, EXT CLOCK SELECT* is asserted to control master clock generator 706 to select the EXT CLOCK input as the source of the clock signal to the divide-by-N counter. Interface circuit between the tester 101 and DUT signal levels of the same design that are discussed below for the response line interface 720 are used to interface the EXT CLOCK signal into the master clock generator 706.

Still referring to FIG. 7(*a*), start test cycle generator 714, in association with the listen enable generator 712, controls the starting and stopping of the test cycle in which the digital test signals are generated and the response line signal monitored by the functional tester 106. Responding to start test cycle generator 714, listen enable generator 712 also generates a listen enable signal LISTEN* that is inputted to the functional tester 106 to allow the functional tester 106 to examine the response line signal 128 when the listen enable signal is true.

FIG. 8 illustrates the circuit diagram for start test cycle generator 714 and the listen enable generator 712. Start test cycle generator 714 generates the signal START CYCLE* to indicate the beginning of a test cycle. Upon the issuance of the system command CMD1*, flip-flop 800 is clocked by MCKL a logic 1 thus enabling one input of NAND gate 814. Because the Q output of flip-flop 800 was at a logic 0 prior to the issuance of CMD1*, the Q* output of flip-flop 802 is at a logic 1 when CMD1* is asserted. This signal is inputted to NAND gate 814 as well as the Q output of flip-flop 800 so that on the occurence of a logic 1 on the Q output of flip-flop 800, the output of NAND gate 814 asserts START CYCLE*. One MCKL cycle later, flip-flop 802 is clocked to a logic zero causing the output of NAND gate 814 to switch back to a logic one. Thus, START CYCLE* is asserted for one clock cycle of MCKL. Following the assertion of START CYCLE*, DCLR* goes true to indicate that a test cycle is occurring. The Q output of flip-flop 802 is DCLR* which assumes a logic 1 state during a test cycle. A test cycle will continue as long as flip-flop 802 is at a logic one. The three signals START CYCLE*, DCLR* and its inverse DCLR are used throughout the digital tester 101 to enable and disable the various functions that are performed.

The listen enable generator 712, as shown in FIG. 8, determines the length of the test cycle and generates a listen enable signal LISTEN* that enables the functional tester 106 to monitor and test the response signal 128 during a test cycle. LISTEN* will be enabled from the first occurrence of a selected pin memory address, although it may not actually be asserted at that time. Further conditions must also occur before LISTEN* will be asserted. To better understand the function of listen enable generator 712, refer to FIG. 10, which illustrates the timing diagram for five possible digital test signals that are members of the set of digital test signals. Each transition in the illustrated waveforms of FIG. 10 occurs when the pin memory address for that test signal occurs (see FIG. 3). Thus, a transition in f_3 occurs when the address "3" occurs. The listen enable generator 712 generates LISTEN* during the time that two preselected test signals are at a logic one and that a first preselected pin memory address has occurred and that a second preselected pin memory address has not. In other words, LISTEN* can occur between the first occurrence of two pin memory addresses but will not be asserted until two other test signals are simultaneously in a logic one state. For example, FIG. 10 illustrates the generation of LISTEN* that is enabled between address 1 and address 4 with the added conditions that f_2 and f_3 are at a logic one.

The signal LISTEN* is generated as follows: Listen enable generator 712, as shown in FIG. 8, has a 16 $\times$4 bit memory 804 which is similar to the memories 214 in pin memory 112 (see FIG. 2(*b*)). Inputted to memory 804 are the pin memory address signals MA0 through MA3. These address signals, as previously discussed, are generated both during the test cycle and also during the initialization of the digital tester 101. Also inputted to memory 804 are write enable and data input lines from CPU 100. During the initialization of the digital tester 101, data on the data lines MD4* through MD7* are strobed into memory 804 by asserting bit 7 of port #1 while the pin memories 112 are being programmed. During the test cycle, the contents of memory 804 are outputted to flip-flops 806, 808, 810 and 812 under control of the Gray Code pinmemory address that are used by memories 214 to generate the digital test signals for the test pins. The J and F inputs to flip-flops 806, 808 and 810 are connected to one of the four output bits from memory 804. The J and K inputs to flip-flop 812 is connected to the output from AND gate 816 that has as one of its two inputs, the last of the four bits from memory 804. This bit is enabled through AND gate 816 by the signal INIT COMPLETE (see FIG. 5) from the test signal address generator 202. INIT COMPLETE goes true at the end of the initialization and preset portion of the test cycle. The signal INIT COMPLETE is used to prevent the addresses which occur during the initialization and preset portion of the test cycle from terminating the test cycle should those addresses be used in the generation of LISTEN*.

The Q ouputs from flip-flop 806 and 808 are inputted to four input AND gate 826 whose output is the signal LISTEN*. The function of flip-flop 806 is to enable one input to AND gate 826 when the first occurence of a pin memory address occurs thereby signifying that one of the possible Gray Code signals has gone to a logic one. The function of flip-flop 808 is the same as 806. The Q output from set-reset flip-flops 820 and 822 are inputted as the two remaining inputs to AND gate 826. Flip-flop 820 is set when flip-flop 810 is clocked to a logic one and flip-flop 822 is reset (flip-flop 822 was set at the start of the test cycle by DCLR*) by the Q output of flip-flop 812 through NAND gate 824 which was enabled by the Q output of flip-flop 820 after flip-flop 820 has been set. In operation, the memory 804 is programmed with logic one's in the appropriate memory locations so that on the occurrence of the pin memory address, during a test cycle, that are selected to start and stop the generation

of the signal LISTEN* during a logic high of any two Gray Code signals, a logic one will be outputted to flip-flops 806, 808, 810 and 812. When flip-flops 806, 808 and 810 have been set, LISTEN* will be asserted. When flip-flop 812 is set, LISTEN* will go false terminating the enable signal to the functional tester 106 and the test cycle will be terminated. The Q output of flip-flop 822, which is reset when flip-flop 812 is set, is the signal STOP CYCLE which is inputted to the start test cycle generator 714 to terminate the test cycle.

Now turning to FIG. 7(*a*), functional tester 106 is shown, composed of response interface 720 responding to the response signal input 128 and the (−) THRESHOLD voltage to generate the response signal RDATA. Also associated with the output of response line interface 720 is an analog-to-digital converter 722, for converting the analog response line signal 128 to an 8 bit digital reresentation. The output of analog-to-digital converter 722 is inputted to CPU 100 through one of the input ports of I/O ports 102 when the analog voltage of the response line is desired. Functional tester 106, in addition to the analog-to-digital converter test, performs three other tests. First, the CRC function tester 724 monitors a bit stream of 1's and 0's on RDATA, to generate a compact digital code representing the length and character of the bit stream. Second and third the COUNT and HIGH function tester 726 counts the number of transistions that occurred in RDATA during the test cycle for a COUNT test, while the HIGH test counts the number of system clocks MCKL that occur during the logic high periods of the response signal RDATA.

Referring now to FIG. 9, which illustrates the circuit diagram of the functional tester 106, the response line signal 128 is shown inputted to buffer amplifier 902 through series resistor 900. The input voltage to buffer 902 is diode limited between +15 volts and analog ground by diodes D_1 and D_2. The output of buffer amplifier 902 is inputtedto resistor 905 and to the analog-to-digital converter 722. The output of buffer amplifier 902 is summed with the (−) THRESHOLD voltage generated by the digital-to-analog converter 702 (see FIG. 7(*a*)), to form the input voltage to comparator 906. Resistors 904 and 905, which are both connected to the input of comparator 906, comprise the summing network which adds the (−) THRESHOLD voltage to the output of buffer 902. Diodes D_3 and D_4 are connected, in parallel but opposite directions, from the input of comparator 906 to analog ground. With this configuration, D4 limits positive voltages while D3 limits negative voltages. In this way, the input voltage to comparator 906 is limited to voltages of a plus or minus one diode drop about the mid-point of the expected response signal swing of the response line 128. The output of comparator 906 is the signal RDATA, which is inputted to the CRC 724 and COUNT and HIGH 726 function testers.

As shown in FIG. 9, CRC function tester 724 uses a CRC generator/checker, such as that manufactured by Fairchild Semiconductor model 9401, described in their 1976 catalog entitled "micro-logic", which catalog is incorporated herein for all purposes. This device generates a cyclic redundancy check code on the signal RDATA. The system clock MCKL, when not inhibited by LISTEN*, clocks CRC generator 724 through NAND gates 908 and NOR gate 910. At the completion of the test cycle, the contents of the CRC generator 724 are clocked into CPU 100 with the assertion of the command CMD8*. Each assertion of CMD8* clocks 1 bit of the cyclic redundancy check code into the CPU 100.

As discussed above, the COUNT and HIGH function tester 726 either counts the number of transitionsin RDATA during the test cycle or counts the number of system clocks during the test cycle when RDATA was true. When the functional test COUNT is true, a cascaded connection of BCD counters 934, 936, 938 and 940 count the number of positive transitions of the response signal RDATA that occurred during the test cycle. The signal COUNT* is ANDED with the signal RDATA through AND gate 930 to generate the clock signal for the BCD counters. When the inhibit signal LISTEN* goes false, the BCD counters are allowed to count. In a similar manner, for the functional test HIGH, NAND gate 932 generates a clock signal to the BCD counters from the system clock MCKL when the signal RDATA is true.

At the completion of both the COUNT and HIGH functional test, the contents of the BCD counters are multiplexed onto a single line and inputted to CPU 100. This multiplexing is accomplished by binary counter 914 and the one-of-four decoders 916 and 918. The outputs from each of the BCD counters are selectively enabled by a select line for each counter. The common outputs from each of the counters may be bussed together, so that only the output of the BCD counter selected will be presented to the bus. System command CMD8* is counted by counter 914, which outputs a 4 bit digital code in which the two lower order bits are inputted to one-of-four decoder 916, to generate four enable signals. The two upper bits are inputted to one-of-four encoder 918 to generate four select signals. The enable signals are inputted to multiplexer NAND gates 920, 922, 924 and 926. The bussed output of each of the BCD counters is inputted as the other input to each of these multiplexer NAND gates. The outputs of the multiplexer NAND 920, 922, 924 and 926 are connected together to form the single output signal COUNT AND HIGH RESULT, which is inputted to the CPU 100 via an input port of I/O ports 102. These multiplexing circuits function so that each assertion CMD8* causes each succeeding output from the four cascaded BCD counters 934, 936, 938 and 940 to be sequentially multiplexed onto the COUNT AND HIGH RESULT signal line.

When the results from the functional tester 106 have been inputted to the CPU 100, routines will be executed to compare the measured result to a result that would be expected from a properly functioning DUT. Based on this comparison, a determination is made as to how the DUT performed.

In describing the invention, reference has been made to a preferred embodiment. However, those skilled in the art and familiar with the disclosure of the invention may recognize additions, deletions, substitutions or other modifications which would fall within the purview of the invention as defined in the appended claims.

What is claimed is:

1. Apparatus for the in-circuit testing of the electrical properties of components of a circuit, comprising:

(a) a central processing unit for controlling the tests to be performed and for interpreting the results of said tests;

(b) electrical test pins, contactable with electrical nodes in said circuit;

(c) sets of selectable switches, one set associated with each of said test pins, for connecting each of said test pins to at least one of a plurality of signal lines associated with each said pin, said signal lines including a response signal line;

(d) a plurality of digital test-signal generators, each of said generators being associated with one of said test pins, for generating at least one digital test signal from a set of test signals, the output line from each of said generators comprising one of the plurality of signal lines for the test pin associated with said generator;

(e) switch-selecting means responsive to the central processor, for selecting at least one of said selectable switches, to connect selected ones of said test pins to their associated plurality of signal lines, thereby to connect one of said plurality of digital test-signal generators to one of the nodes of the circuit, and to connect a node of the circuit to the response signal line;

(f) a test controller responsive to the central processor, for generating a test cycle wherein said digital test-signal generators supply test signals to said circuit, thereby to cause the circuit to produce a response signal on said response signal line; and

(g) a functional tester responsive to the central processor, for testing the signal on said response signal line, to determine electrical properties of said circuit.

2. The apparatus in accordance with claim 1 wherein said electrical test pins comprise a bed of nails fixture.

3. The apparatus of claim 1, wherein the plurality of selectable switches in each of said sets of selectable switches includes four selectable switches.

4. The apparatus of claim 1, wherein said selectable switches are reed switches.

5. The apparatus of claim 1, wherein said set of test signals includes a set of Gray Code test signals.

6. The apparatus of claim 5 wherein, the set of Gray Code test signals comprises fourteen digital test signals.

7. The apparatus of claim 1, wherein each of said digital test-signal generators includes:

(a) a memory address generator for generating a sequence of memory addresses during said test cycle;

(b) a first memory responsive to said address generator, for outputting a logic signal to select a digital test signal, said memory having a specified storage location for each digital test signal, said logic signal enabling a transition in said selected test signal;

(c) a second memory responsive to said address generator, for outputting a logic signal to enable and to disable the generation of said selected test signal;

(d) a synchronization signal generator responsive to said memory address generator for generating synchronization signals; and

(e) a driver responsive to the output from said first and second memories, and to said synchronization signals, for generating the selected digital test signal and for applying said selected digital test signal to an electrical node of said circuit.

8. The apparatus of claim 7, wherein said sequence of memory addresses comprises the ordered sequential addresses of each of the addressable storage locations of said first memory and said second memory, each address in said sequence enabling a transition in said digital test signal specified by that address.

9. The apparatus of claim 8, wherein said first memory further comprises a memory location for storing an initialization bit, and another memory location for storing a preset bit, said initialization and preset bits specifying one of a plurality of possible beginning sequences for each of said digital test signals.

10. The apparatus of claim 7, wherein said synchronization signal generator includes:

(a) means for generating a first synchronization signal having a transition for each address of said address generator; and

(b) means for generating a second synchronization signal having a transition,

(i) on the first occurrence of each address in said sequence of memory addresses, or

(ii) on each occurrence of any or all addresses in said sequence of memory addresses.

11. The apparatus of claim 7, wherein said digital test signal generator further comprises means responsive to said processor for addressing and storing in said first and second memories digital-test-signal-generating data prior to the generation of said test cycle.

12. The apparatus of claim 1, wherein said test controller includes:

(a) an internal oscillator;

(b) a threshold voltage generator responsive to said processor for generating a negative offset voltage to offset the voltages produced by externally generated signals inputted to the testing apparatus, the external signals including an external clock signal;

(c) a system clock generator responsive to the external clock signal, said processor, said oscillator and said threshold voltage generator, for generating a system clock, said system clock being derived from said internal oscillator or from the external clock;

(d) a command decoder responsive to said processor, for generating system commands to control the functions of said tester;

(e) a listen enable generator responsive to said processor and said digital test-signal generators, for controlling the length of said test cycle, and for generating a listen enable signal to enable said functional tester to perform functional tests on said response signal during the generation of said listen enable signal; and

(f) a start test cycle generator responsive to said clock, said listen enable generator, and said command decoder, for starting and stopping said test cycle.

13. The apparatus of claim 12, wherein said system clock generator includes a divide-by-N counter.

14. The device of claim 12, wherein said threshold voltage generator is a digital-to-analog converter.

15. The apparatus of claim 1, wherein said functional tester includes a cyclic redundancy check function tester for generating a digital code representative of the length and character of the serial digital data stream of said response signal, said code representing the signature of said response signal.

16. A testing apparatus adapted for use with a computer for the in-circuit testing of a circuit having electrical nodes, comprising:

(a) a node-connecting means associated with each of a selected ones of said nodes and responsive to the computer, each selected node having associated therewith signal lines including a response signal line, for connecting each of the selected nodes to its associated signal lines, one of said selected nodes being connected to the response signal line;

(b) a digital test-signal generator associated with each said node-connecting means, for generating at least one digital test signal from a set of digital test signals, the output line from each said generator comprising one of the associated signal lines for the node associated with said generator;

(c) a controller responsive to the computer, for generating a test cycle in which selected ones of said test signals are applied through said associated node-connecting means to selected ones of said selected nodes, said circuit generating a signal on said response signal line in response to said applied test signals; and

(d) a functional tester connected to the response signal line and responsive to the computer, for performing functional tests on said response signal to determine electrical properties of said circuit.

17. The apparatus of claim **16**, wherein each said node-connecting means includes:

(a) a test pin contactable with an associated selected electrical node of said circuit; and

(b) a set of selectable switches connected to each of said test pins, for connecting each test pin to one of its associated signal lines; and

(c) switch selecting means responsive to the computer, for selecting at least one of said selectable switches,

(i) to connect one of said plurality of digital test-signal generators to one of the nodes of the circuit, and

(ii) to connect a node of the circuit to the response signal line.

18. The apparatus of claim **17**, wherein each said set of selectable switches includes a switch for connecting the output from one of said associated digital test-signal generators to its associated test pin.

19. The apparatus in accordance with claim **16**, wherein said functional tester includes:

(a) an analog-to-digital converter;

(b) a counter for counting

(i) the number of cycles in a clock signal that occurred when said response test signal is at a logic high state, or

(ii) the number of pulses in said response test signal that occur in said test cycle; and

(c) a cyclic redundancy check generator, for generating a digital code for the serial bit stream of said response test signal, said code representing the signature of said signal.

20. The apparatus of claim **16**, wherein said controller includes:

(a) a system clock generator responsive to said computer for generating a master system clock for said tester;

(b) a command decoder responsive to said computer for generating control signals to control the functions of said tester;

(c) a listen enable generator responsive to said computer and said digital test-signal generators, for generating a listen enable signal, to enable said functional tester to perform functional tests on said response signal during the generation of said listen enable signal, and for controlling the length of said test cycle; and

(d) a start test cycle generator responsive to said system clock, said command decoder and said listen enable generator, for starting the stoping said test cycle.

21. Apparatus adapted for use with a central processor for the in-circuit testing of the electrical properties of a circuit under test, said apparatus having a response signal line for monitoring the response signal from the circuit under test, the apparatus comprising:

(a) electrical test pins, contactable with electrical nodes in said circuit;

(b) a selectable switch associated with each test pin, for selectively connecting the associated said test pin to the response signal line;

(c) a plurality of digital test-signal generators, one associated with each of said test pins, for generating at least one digital test signal from a set of test signals, the output line from each said generator adapted for connection to its associated test pin;

(d) switch-selecting means responsive to the central processor, for selecting one said selectable switch to connect a node of said circuit to said response signal line; and

(e) a test controller responsive to the central processor, for generating a test cycle wherein selected ones of said digital test-signal generators supply test signals to said circuit, thereby to cause the circuit under test to produce a response signal on said response signal line.

22. The apparatus in accordance with claim **21** further comprising a functional tester connected to the response signal line and responsive to the central processor, for testing the signal on the response signal line, to determine electrical properties of the circuit.

23. The apparatus in accordance with claim **21** wherein said electrical test pins comprise a bed of nails fixture.

24. The apparatus of claim **21**, wherein said selectable switch is a reed switch.

25. The apparatus of claim **21**, wherein the set of test signals includes a set of Gray Code test signals.

26. The apparatus of claim **25**, wherein the set of Gray Code test signals comprises fourteen digital test signals.

27. The apparatus of claim **21**, wherein each of said digital test-signal generators includes:

(a) a memory address generator for generating a sequence of memory addresses during said test cycle;

(b) a first memory responsive to said address generator, for outputting a logic signal to select a digital test signal , said memory having a specified storage location for each digital test signal, said logic signal enabling a transition in said selected test signal;

(c) a second memory responsive to said address generator, for outputting a logic signal to enable and to disable the generation of said selected test signal;

(d) a synchronization signal generator responsive to said memory address generator for generating synchronization signals; and

(e) a driver responsive to the output from said first and second memories, and to said synchronization signals, for generating the selected digital test signal and for applying said selected digital test signal to an electrical node of said circuit.

28. The apparatus of claim **27**, wherein said sequence of memory addresses comprises the ordered sequential addresses of each of the addressable storage locations of said first memory and said second memory, each address in said sequence enabling a transition in said digital test signal specified by that address.

29. The apparatus of claim **28**, wherein said first memory further comprises a memory location for storing an

initialization bit, and another memory location for storing a preset bit, said initialization and preset bits specifying one of a plurality of possible beginning sequence for each of said digital test signals.

30. The apparatus of claim 27, wherein said synchronization signal generator includes:

(a) means for generating a first synchronization signal having a transition for each address of said address generator; and

(b) means for generating a second synchronization signal having a transition,

(i) on the first occurrence of each address in said sequence of memory addresses, or

(ii) on each occurrence of any or all addresses in said sequence of memory addresses.

31. The apparatus of claim 27, wherein said digital test signal generator futher comprises means responsive to said processor for addressing and storing in said first and second memories digital-test-signal-generating data prior to the generation of said test cycle.

32. The apparatus of claim 22, wherein said test controller includes:

(a) an internal oscillator;

(b) a threshold voltage generator responsive to said processor for generating a negative offset voltage to offset the voltages produced by externally generated signals inputted to the testing apparatus, said external signals including an external clock signal;

(c) a system clock generator responsive to the external clock signal, said processor, said oscillator and said threshold voltage generator, for generating a system clock, said system clock being derived from said internal oscillator or from the external clock;

(d) a command decoder responsive to said processor, for generating system commands to control the functions of said tester;

(e) a listen enable generator responsive to said processor and said digital test-signal generator, for controlling the length of said test cycle, and for generating a listen enable signal to enable said functional tester to perform functional tests on said response signal during the generation of said listen enable signal; and

(f) a start test cycle generator responsive to said listen enable generator, for starting and stopping said test cycle.

33. The apparatus of claim 32, wherein said system clock generator includes a divide-by-N counter.

34. The device of claim 32, wherein said threshold voltage generator is a digital-to-analog converter.

35. The apparatus in accordance with claim 22, wherein said functional tester includes:

(a) an analog-to-digital converter;

(b) a counter for counting

(i) the number of cycles in a clock signal that occurred when said response signal is at a logic high state, or

(ii) the number of pulses in said response signal that occur in said test cycle; and

(c) a cyclic redundancy check generator, for generating a digital code from the serial bit stream of said response signal, said code representing the signature of said signal.

36. An apparatus for use with a central processing unit for in-circuit testing of the electrical properties of components of a circuit, said apparatus comprising:

(a) electrical test pins, contactable with electrical nodes in said circuit;

(b) sets of selectable switches, one set associated with each of said test pins, for connecting each of said test pins to at least one of a plurality of signal lines associated with each said pin, said signal lines including a response signal line;

(c) a plurality of digital test-signal generators, each of said generators being associated with one of said test pins, for generating at least one digital test signal, the output line from each of said generators comprising one of the plurality of signal lines for the test pin associated with said generator;

(d) switch selecting means responsive to the central processor, for selecting at least one of said selectable switches, to connect selected ones of said test pins to their associated plurality of signal lines, thereby

(i) to connect one of said plurality of digital test-signal generators to one of the nodes of the circuit, and

(ii) to connect a node of the circuit to the response signal line; and

(e) a test controller responsive to the central processor, for generating a test cycle wherein said digital test-signal generators supply test signals to said circuit, thereby to produce a response signal on said response signal line.

37. The apparatus according to claim 36 further comprising a functional tester responsive to the central processor, for testing the signal on said response signal line, to determine electrical properties of the components of said circuit.

38. The apparatus in accordance with claim 36 wherein said electrical test pins comprise a bed of nails fixture.

39. The apparatus of claim 36, wherein each of said sets of selectable switches includes four selectable switches.

40. The apparatus of claim 36, wherein said selectable switches are reed switches.

41. The apparatus of claim 36, wherein said set of test signals includes a set of Gray Code test signals.

42. The apparatus of claim 41 wherein, the set of Gray Code test signals comprises fourteen digital test signals.

43. The apparatus of claim 36, wherein each of said digital test-signal generators includes:

(a) a memory address generator for generating a sequence of memory addresses during said test cycle;

(b) a first memory responsive to said address generator, for outputting a logic signal to select a digital test signal, said memory having a specified storage location for each digital test signal, said logic signal enabling a transition in said selected test signal;

(c) a second memory responsive to said address generator, for outputting a logic signal to enable and to disable the generation of said selected test signal;

(d) a synchronization signal generator responsive to said memory address generator for generating synchronization signals; and

(e) a driver responsive to the output from said first and second memories, and to said synchronization signals, for generating the selected digital test signal and for applying said selected digital test signal to an electrical node of said circuit.

44. The apparatus of claim 43, wherein said sequence of memory addresses comprises the ordered sequential addresses of each of the addressable storage locations of said first memory and said second memory, each ad-

dress in said sequence enabling a transition in said digital test signal specified by that address.

45. The apparatus of claim 44, wherein said first memory further comprises a memory location for storing an initialization bit, and another memory location for storing a preset bit, said initialization and preset bits specifying one of a plurality of possible beginning sequences for each of said digital test signals.

46. The apparatus of claim 43, wherein said synchronization signal generator includes:

(a) means for generating a first synchronization signal having a transition for each address of said address generator; and

(b) means for generating a second synchronization signal having a transition,

(i) on the first occurrence of each address in said sequence of memory addresses, or

(ii) on each occurrence of any or all addresses in said sequence of memory addresses.

47. The apparatus of claim 43, wherein said digital test signal generator further comprises means responsive to said processor for addressing and storing in said first and second memories digital-test-signal-generating data prior to the generation of said test cycle.

48. The apparatus of claim 37, wherein said test controller includes:

(a) an internal oscillator;

(b) a threshold voltage generator responsive to said processor for generating a negative offset voltage to offset the voltages produced by externally generated signals inputted to the testing apparatus;

(c) a system clock generator responsive to an external clock signal, said processor, said oscillator and said threshold voltage generator, for generating a system clock, said system clock being derived from said internal oscillator or from the external clock;

(d) a command decoder responsive to said processor, for generating system commands to control the functions of said tester;

(e) a listen enable generator responsive to said processor and said digital test-signal generators, for controlling the length of said test cycle, and for generating a listen enable signal to enable said functional tester to perform functional tests on said response signal during the generator of said listen enable signal; and

(f) a start test cycle generator responsive to said system clock, said listen enable generator, and said command decoder, for starting and stopping said test cycle.

49. The apparatus of claim 48, wherein said system clock generator includes a divide-by-N counter.

50. The device of claims 48, wherein said threshold voltage generator is a digital-to-analog converter.

51. The apparatus of claim 37, wherein said functional tester includes a cyclic redundancy check function tester for generating a digital code representative of the length and character of the serial digital data stream of said response signal, said code representing the signature of said response signal.

52. An in-circuit testing apparatus adapted for use with a computer for the in-circuit testing of the electrical properties of components in the circuit, the circuit having electrical nodes at which the components are interconnected, the apparatus comprising:

(a) means associated with each of selected nodes, and responsive to the computer, for connecting each selected node to one of a plurality of signal lines associated with each selected node, each plurality of signal lines including a response signal line;

(b) a digital test-signal generator associated with each said means, for generating a digital test signal for the circuit under test, the output line from each said generator comprising one of the associated signal lines for the node associated with said generator, said means

(i) connecting one of said digital test-signal generators to a selected node, and

(ii) connecting a selected node to the response signal line; and

(c) a test controller responsive to the computer, for generating a test cycle in which digital test signals are applied to selected nodes, the circuit generating a signal on the response signal line in response to the applied test signals.

53. The apparatus according to claim 52 further comprising a functional tester for performing functional tests on said response signal to determine electrical properties of the components of the circuit.

54. The apparatus of claim 52, wherein said means includes:

(a) a test pin contactable with an associated selected electrical node of the circuit;

(b) a set of selectable switches connected to each of said test pins, for connecting each test pin to one of its associated signal lines; and

(c) switch selecting means responsive to the computer, for selecting said selectable switches.

55. The apparatus of claim 54, wherein each said set of selectable switches includes a switch for connecting the output from one of said associated digital test-signal generators to its associated test pin.

56. The apparatus in accordance with claim 53, wherein said functional tester includes:

(a) an analog-to-digital converter;

(b) a counter for counting

(i) the number of cycles in a clock signal that occurred when said response signal is at a logic high state, or

(ii) the number of pulses in said response signal that occur in said test cycle; and

(c) a cyclic redundancy check generator, for generating a digital code from the serial bit stream of said response signal, said code representing the signature of said signal.

57. The apparatus of claim 52, wherein said controller includes:

(a) a system clock generator responsive to said computer for generating a master system clock for said tester;

(b) a command decoder responsive to said computer for generating control signals to control the functions of said tester;

(c) a listen enable generator responsive to said computer and said digital test-signal generators, for generating a listen enable signal, to enable said functional tester to perform functional tests on said response signal during the generation of said listen enable signal, and for controlling the length of said test cycle; and

(d) a start test cycle generator responsive to said system clock, said command decoder and said listen enable generator, for starting and stoping said test cycle.

58. The apparatus of claim 54 wherein the set of selectable switches comprises a single switch which selec-

tively connects its associated test pin to the response signal line, the output from each said test-signal generator being removably connected to its associated test pin whereby the associated test pin connected to the response signal line functions alternatively

(a) as an input stimulus point to the circuit under test during the entire test cycle, or

(b) as an input stimulus point for a first portion of the test cycle, and as an output response signal point for a second portion of the test cycle.

59. Apparatus adapted for use with a central processor for the in-circuit testing of the electrical properties of components of a circuit under test, said apparatus having a response signal line for monitoring the response signal from the circuit under test, the apparatus comprising:

(a) electrical test pins, contactable with electrical nodes in the circuit;

(b) a selectable switch associated with each test pin, for selectively connecting the associated said test pin to the response signal line;

(c) a plurality of digital test-signal generators, one associated with each of said test pins, for generating at least one digital test signal from a set of test signals, the output line from each said generator adapted for connection to its associated test pin, each said digital test-signal generator including,

(i) a memory address generator for generating a sequence of memory addresses during said test cycle,

(ii) a first memory responsive to said address generator, for outputting a logic signal to select a digital test signal, said memory having a specified storage location for each digital test signal, said logic signal enabling a transition in said selected test signal,

(iii) a second memory responsive to said address generator, for outputting a logic signal to enable and to disable the generation of said selected test signal,

(iv) a synchronization signal generator responsive to said memory address generator for generating synchronization signals, and

(v) a driver responsive to the output from said first and second memories, and to said synchronization signals, for generating the selected digital test signal and for applying said selected digital test signal to an electrical node of said circuit;

(d) switch-selecting means responsive to the central processor, for selecting one said selectable switch to connect a node of said circuit to said response signal line;

(e) a test controller responsive to the central processor, for generating a test cycle wherein selected ones of said digital test-signal generators supply test signals to said circuit, thereby to cause the circuit under test to produce a response signal on said response signal line; and

(f) a functional tester connected to the response signal line and responsive to the central processor, for testing the signal on the response signal line, to determine electrical properties of the components of the circuit, said functional tester including,

(i) an analog-to-digital converter,

(ii) a counter for counting

(1) the number of cycles in a clock signal that occurred when said response signal is at a logic high state, or

(2) the number of pulses in said response signal that occur in said test cycle, and

(iii) a cyclic redundancy check generator, for generating a digital code from the serial bit stream of said response signal, said code representing the signature of said response signal.

60. The apparatus of claim 59 wherein said selectable switch selectively connects its associated test pin to the response signal line, the output from each said test-signal generator being removably connected to its associated test pin, whereby the associated test pin connected to the response signal line functions alternatively

(a) as an input stimulus point to the circuit under test during the entire test cycle, or

(b) as an input stimulus point for a first portion of the test cycle, and as an output response point for a second portion of the test cycle.

* * * * *

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(12) **United States Patent**
Mori et al.

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(45) **Date of Patent: Feb. 10, 2004**

(54) **APPARATUS AND METHOD FOR TESTING SEMICONDUCTOR INTEGRATED CIRCUIT**

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(73) Assignees: **Renesas Technology Corp.**, Tokyo (JP); **Ryoden Semiconductor System Engineering Corporation**, Hyogo (JP)

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(52) **U.S. Cl.** **324/765**; 324/763; 324/158.1; 714/733; 714/734

(58) **Field of Search** 324/158.1, 754–765; 714/724–734

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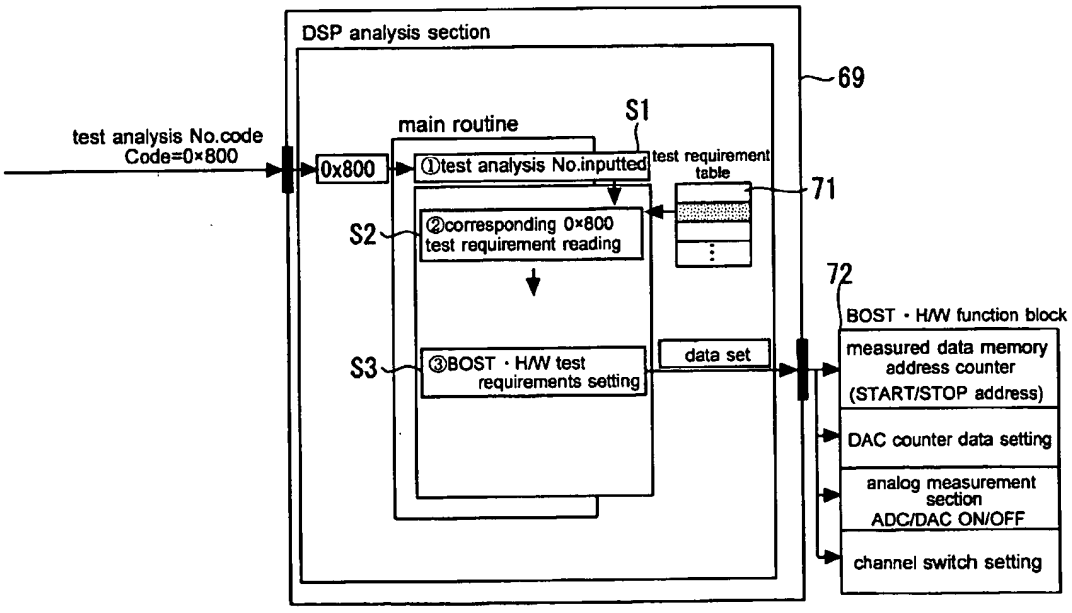
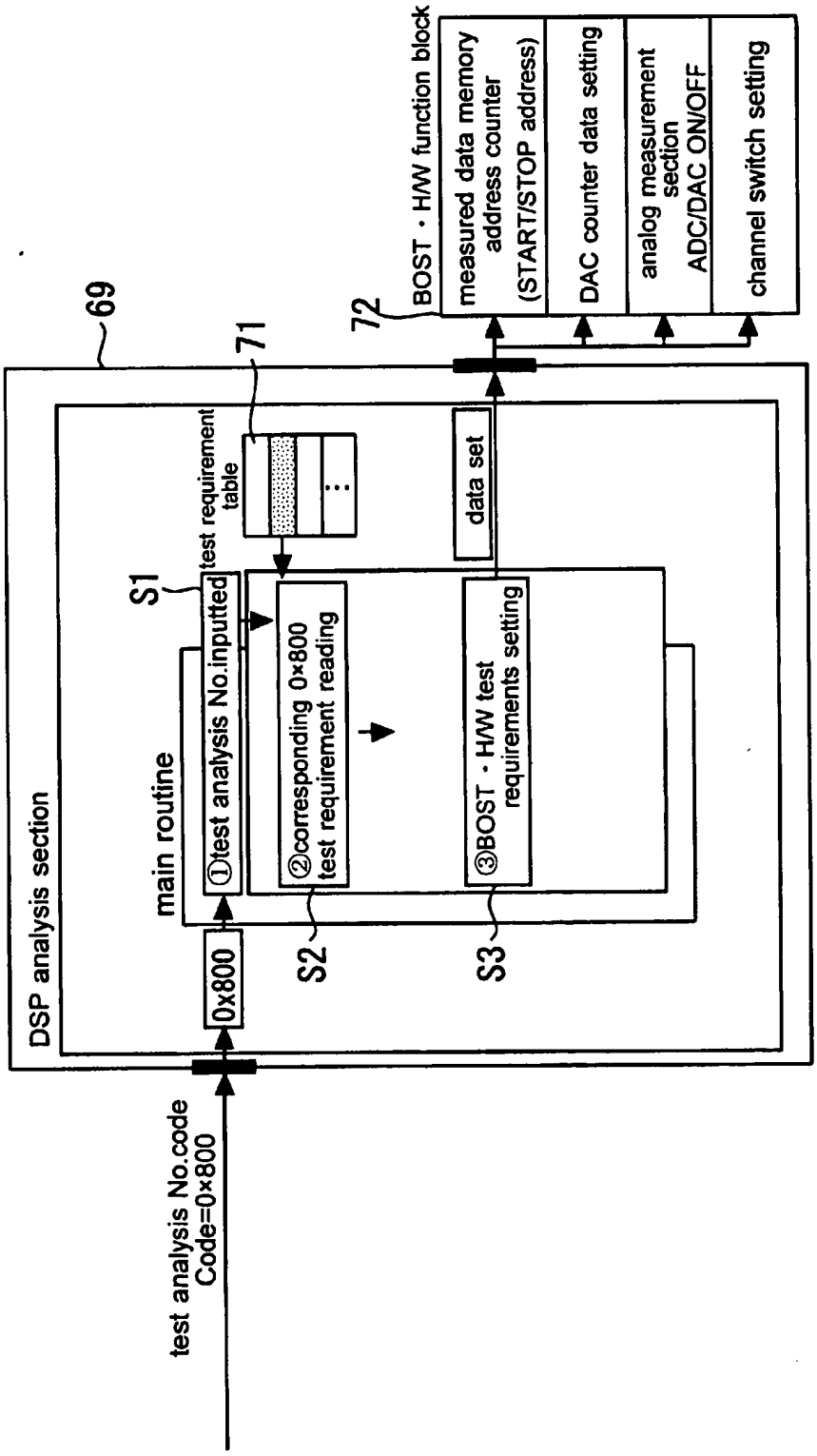
Primary Examiner—Kamand Cuneo
Assistant Examiner—Emily Y Chan
(74) *Attorney, Agent, or Firm*—McDermott, Will & Emery

(57) **ABSTRACT**

There are provided a test apparatus and method for testing a semiconductor integrated circuit which enables improvements in the ease of operation and convenience of a BOST device and shortening of a test time. Numeric codes are assigned to tests. A test apparatus is equipped with memory and an analysis section. A test requirement table—in which hardware requirements required for conducting a test are set on a per-numeric-code basis—is stored in the memory. Test requirements corresponding to a numeric code are read from the memory, whereupon a test is performed. The analysis section analyzes a digital test output and sends the result of analysis to an external controller.

8 Claims, 7 Drawing Sheets

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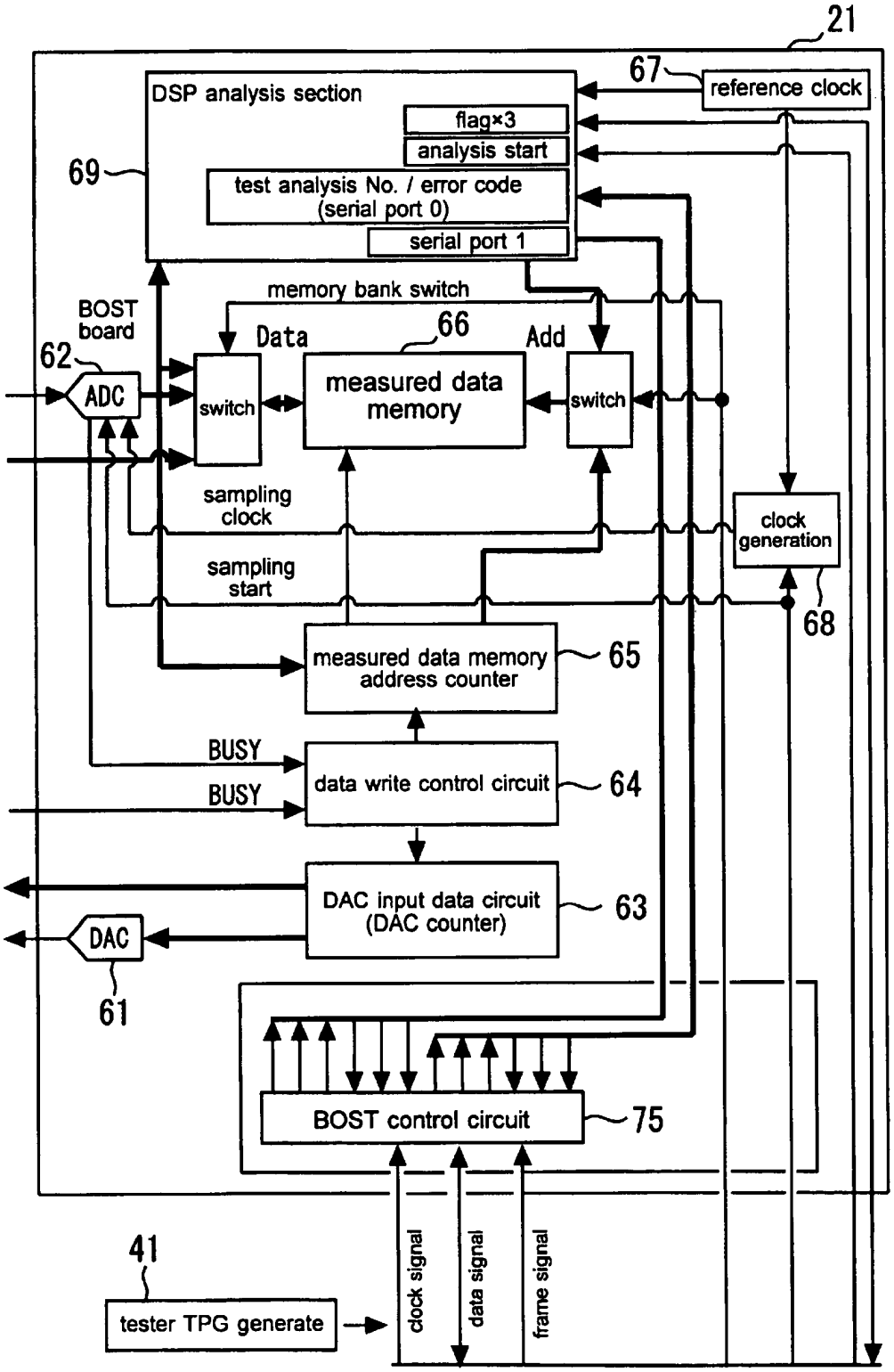
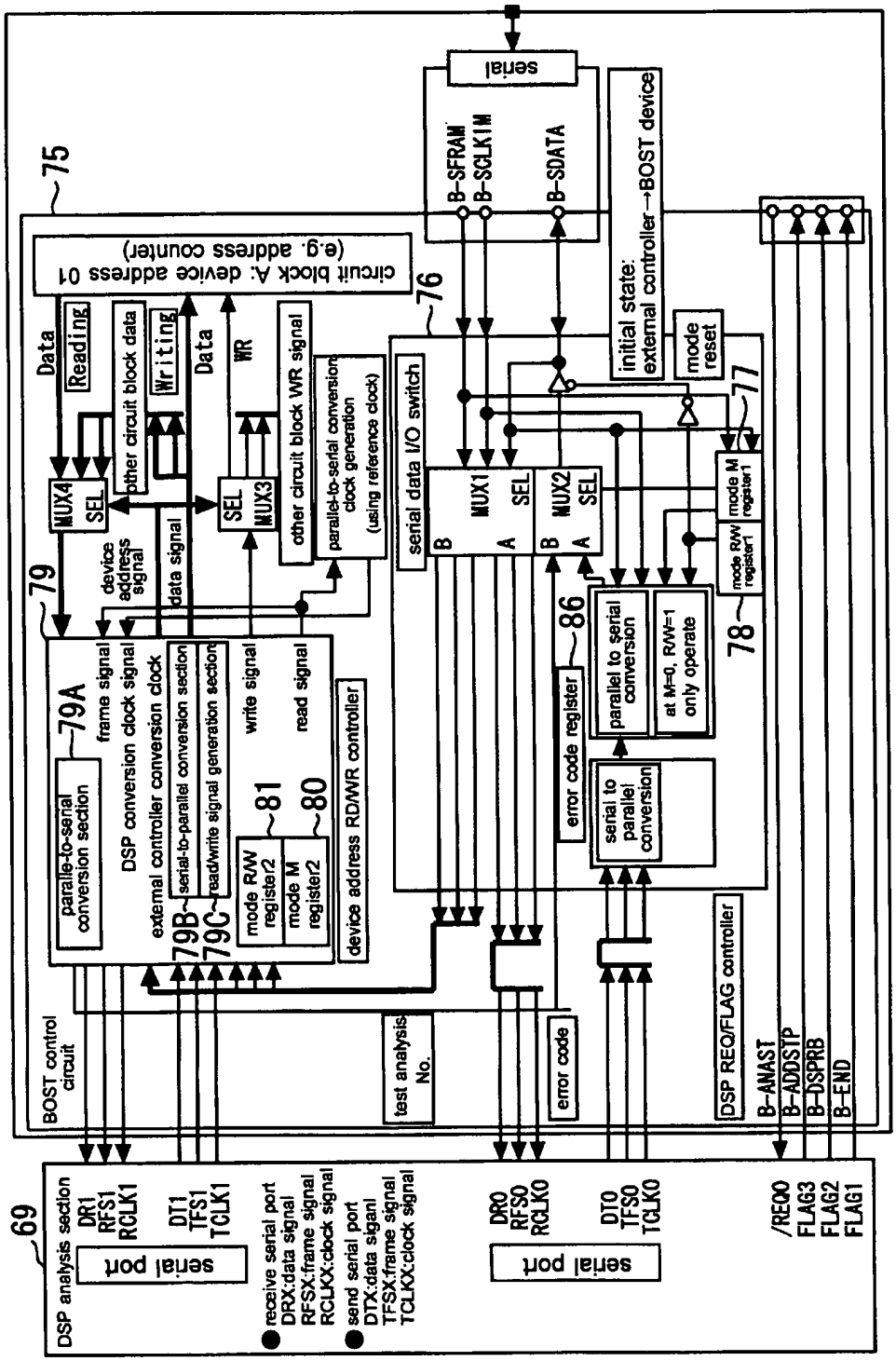
DSP analysis section
69
0x800
main routine
①test analysis No.inputted
S1
test requirement table
71
②corresponding 0x800 test requirement reading
S2
③BOST・H/W test requirements setting
S3
data set
72
BOST・H/W function block
measured data memory address counter (START/STOP address)
DAC counter data setting
analog measurement section ADC/DAC ON/OFF
channel switch setting

Fig. 1

Fig. 2


21
67
reference clock
DSP analysis section
flag×3
analysis start
69
test analysis No. / error code (serial port 0)
serial port 1
memory bank switch
BOST board
Data
66
Add
62
ADC
switch
measured data memory
switch
sampling clock
clock generation
sampling start
68
measured data memory address counter
65
BUSY
BUSY
data write control circuit
64
DAC input data circuit (DAC counter)
63
DAC
61
BOST control circuit
75
41
tester TPG generate
clock signal
data signal
frame signal


75
serial
B-SFRAM
B-SCLK1M
B-SDATA
initial state: external controller→BOST device
mode reset
77
circuit block A: device address 01 (e.g. address counter)
76
Data
Reading
other circuit block data
Writing
Data
WR
other circuit block WR signal
parallel-to-serial conversion clock generation (using reference clock)
serial data I/O switch
MUX4
SEL
MUX3
MUX1
MUX2
mode M register1
mode R/W register1
device address signal
data signal
79
79A
parallel-to-serial conversion section
frame signal
DSP conversion clock signal
external controller conversion clock
serial-to-parallel conversion section
read/write signal generation section
write signal
read signal
79B
79C
mode R/W register2
mode M register2
81
80
device address RD/WR controller
86
error code register
parallel to serial conversion
at M=0, R/W=1 only operate
78
serial to parallel conversion
BOST control circuit
test analysis No.
error code
DSP REQ/FLAG controller
B-ANAST
B-ADDSTP
B-DSPRB
B-END
69
DSP analysis section
serial port
DR1
RFS1
RCLK1
DT1
TFS1
TCLK1
receive serial port
DRX:data signal
RFSX:frame signal
RCLKX:clock signal
send serial port
DTX:data signal
TFSX:frame signal
TCLKX:clock signal
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RCLK0
DT0
TFS0
TCLK0
/REQ0
FLAG3
FLAG2
FLAG1

Fig. 3

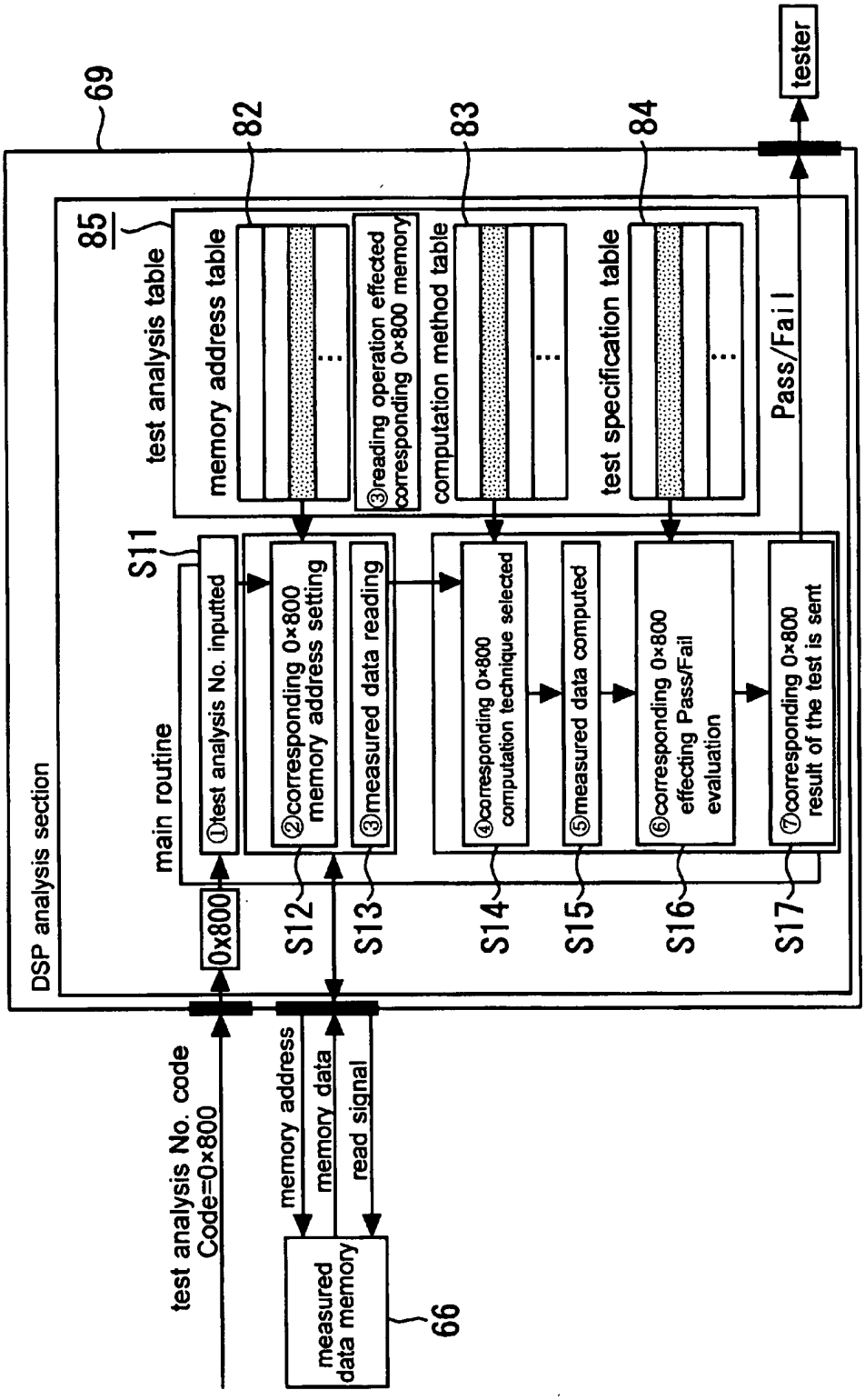
69
82
83
84
tester
85
test analysis table
memory address table
③reading operation effected corresponding 0×800 memory
computation method table
test specification table
Pass/Fail
S11
main routine
①test analysis No. inputted
②corresponding 0×800 memory address setting
③measured data reading
④corresponding 0×800 computation technique selected
⑤measured data computed
⑥corresponding 0×800 effecting Pass/Fail evaluation
⑦corresponding 0×800 result of the test is sent
DSP analysis section
0×800
S12
S13
S14
S15
S16
S17
test analysis No. code Code=0×800
memory address
memory data
read signal
measured data memory
66

Fig. 4

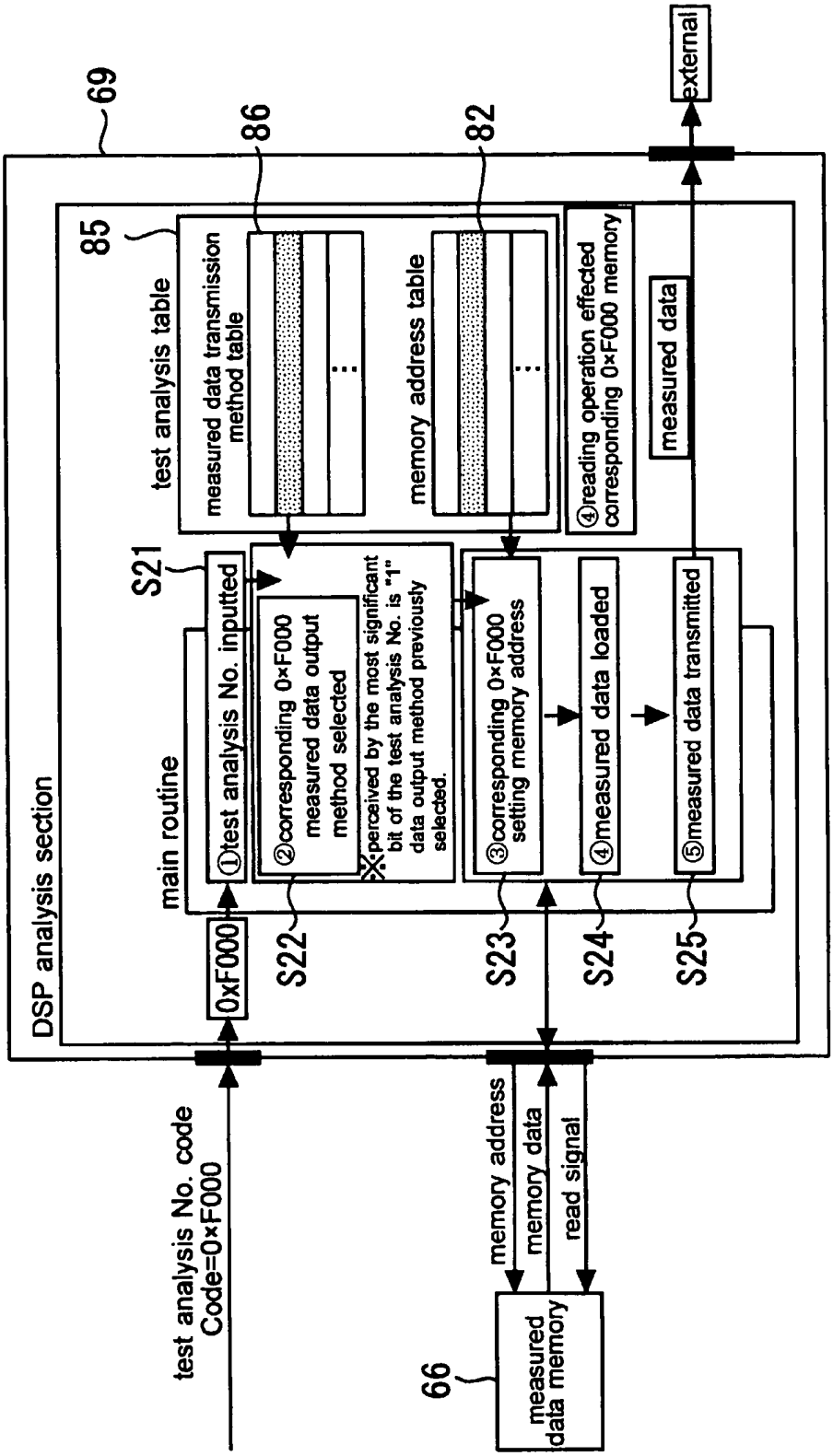
69
86
82
external
85
test analysis table
measured data transmission method table
memory address table
④reading operation effected corresponding 0×F000 memory
measured data
S21
①test analysis No. inputted
②corresponding 0×F000 measured data output method selected
※perceived by the most significant bit of the test analysis No. is "1" data output method previously selected.
③corresponding 0×F000 setting memory address
④measured data loaded
⑤measured data transmitted
main routine
DSP analysis section
0xF000
S22
S23
S24
S25
test analysis No. code Code=0×F000
memory address
memory data
read signal
66
measured data memory

Fig. 5

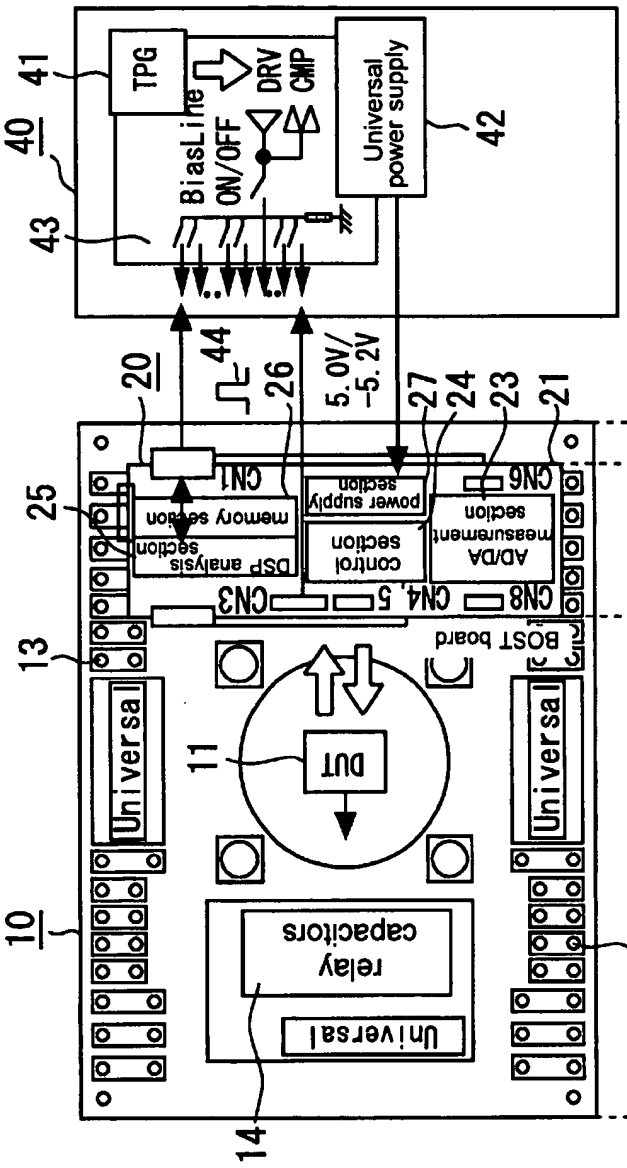

Fig. 6A

Fig. 6B

Fig. 6C

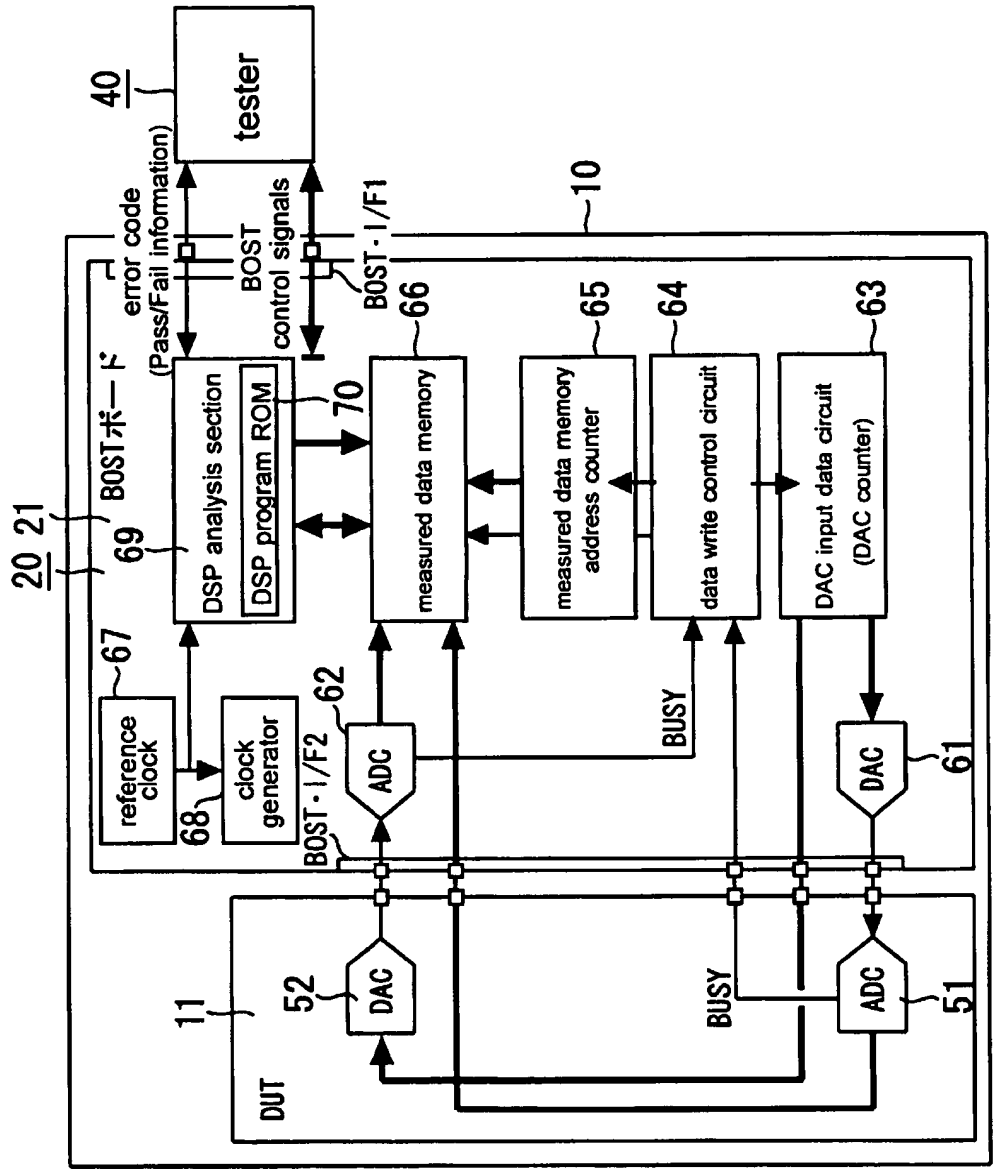
40
tester
error code
(Pass/Fail information)
BOST
control signals
BOST-I/F1
10
20 21
BOSTボード
69
DSP analysis section
DSP program ROM
70
66
measured data memory
65
measured data memory
address counter
64
data write control circuit
63
DAC input data circuit
(DAC counter)
67
reference clock
68
clock generator
BOST-I/F2
62
ADC
BUSY
DAC
61
11
52
DAC
DUT
BUSY
ADC
51

Fig. 7

APPARATUS AND METHOD FOR TESTING SEMICONDUCTOR INTEGRATED CIRCUIT

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to an apparatus for testing a semiconductor integrated circuit, and more particularly to an apparatus and method for testing a semiconductor integrated circuit including an A/D (analog-to-digital) converter circuit for converting an analog signal into a digital signal and a D/A (digital-to-analog) converter circuit for converting a digital signal into an analog signal.

2. Background Art

Recently, in relation to a system LSI embodied in a one-chip semiconductor integrated circuit (a one-chip LSI) consisting of a plurality of functionally-systematized circuit modules or embodied in a hybrid integrated circuit (a chip set LSI), combination of high-performance and precision digital and analog circuits (i.e., a system LSI handling a mixed signal) has been rapidly pursued. Even in relation to a test apparatus for use with a semiconductor integrated circuit, development of a test apparatus capable of handling a mixed signal is also pursued. Tester manufacturers have provided testers coping with a semiconductor integrated circuit using a mixed signal.

A tester compatible with a semiconductor integrated circuit using a mixed signal has a tendency to become expensive in the course of ensuring compliance with high performance specifications. For this reason, moves are afoot to recycle an existing low-speed, low-precision tester which has been used for, e.g., a logic LSI, to thereby avoid a hike in the price of a tester.

A big problem with such a test apparatus lies in a characteristic test for a D/A converter circuit for converting a digital signal into an analog signal (digital-to-analog converter, hereinafter called a "DAC") as well as in a characteristic test for an A/D converter circuit for converting an analog signal into a digital signal (hereinafter called an "ADC"). In association with an increase in the precision of the characteristic test, embodiment of a low-cost test apparatus compatible with a semiconductor integrated circuit including the DAC and ADC has posed a challenge.

In a testing environment of a general tester, a plurality of DUT (device under test) circuit boards (simply called "DUT boards") and connection jigs for connecting a tester with a DUT, such as cables, are provided at a plurality of points along a measurement path extending from measurement equipment provided in the tester to a semiconductor integrated circuit under test (hereinafter called a "DUT"). Further, the measurement path is long and accounts for occurrence of noise and a drop in measurement accuracy. Further, simultaneous testing of a plurality of DUTs is also impossible. A limitation is imposed on the speed of a low-speed tester, and hence the low-speed tester cannot conduct a test at a real operating speed, thereby posing a fear of an increase in a time required for conducting mass-production testing of a system LSI.

Japanese Patent Application Laid-Open No. 316024/1989 describes a tester. The tester is equipped with a memory device for storing conversion data at an address designated by input data which have been entered into a DAC of a test circuit. An analog signal which has been subjected to digital-to-analog conversion is inputted to an ADC, and an output from the ADC is sequentially stored in the memory device. After conversion of all the input data sets has been completed, the conversion data stored in the memory device are sequentially delivered to a tester. The tester sequentially compares the input data with the conversion data, thus producing a test conclusion.

However, the tester must supply data to be inputted to the DAC, an address to be used for storing conversion data into a memory device, and a control signal. Moreover, data stored in the memory device must be supplied to the tester. Further, there is the probability that noise arising in a long measurement path extending from the tester to a DUT may deteriorate precision of measurement. Further, the majority of pin electronics provided on the tester are occupied for testing a single DUT, thereby posing a difficulty in simultaneous measurement of a plurality of DUTs.

Further, communication for transmitting conversion data to the tester is time consuming, and test conclusions are produced after completion of all tests. Hence, shortening of a test time is also difficult.

SUMMARY OF THE INVENTION

The present invention has been conceived to solve such a problem and is aimed at providing an apparatus and method of testing a semiconductor integrated circuit, which apparatus and method facilitate operation of a BOST device and improve the convenience thereof.

According to one aspect of the present invention, an apparatus for testing a semiconductor integrated circuit comprises a test circuit board configured to transmit signals to and receive signals from a semiconductor integrated circuit to be tested that comprises an A/D converter circuit to convert analog signals to digital signals and a D/A converter circuit to convert digital signals to analog signals, a test ancillary device which is disposed in the vicinity of the test circuit board and is connected to the test circuit board, and an external controller which assigns a numeric code to a test on the semiconductor integrated circuit to be performed by the test ancillary device and which transmits the numeric code to the test ancillary device. The test ancillary device comprises memory having stored therein a test requirement table in which hardware requirements required for conducting a test are set on a per-numeric-code, an analysis section for reading test requirements corresponding to the numeric code from the test requirement table; a data circuit which supplies a digital test signal to the D/A converter circuit of the semiconductor integrated circuit to be tested on the basis of the test requirements, a testing D/A converter circuit which converts the digital test signal from the data circuit into an analog test signal and supplies the analog test signal to the A/D converter circuit of the semiconductor integrated circuit to be tested, a testing A/D converter circuit which converts an analog test output from the D/A converter circuit of the semiconductor integrated circuit to be tested into a digital test output, and measured data memory for storing a digital test output from the A/D converter circuit of the semiconductor integrated circuit to be tested and the digital test output from the testing A/D converter circuit. A result of analysis of the each digital test outputs stored in the measured data memory, the analysis being performed by the analysis section, is sent to the external controller.

By means of the test apparatus and the test method according to the present invention, numeric codes are assigned to tests to be performed by a DUT. The test apparatus is equipped with memory, and a test requirement table having stored therein specification evaluation values

stored therein. A test requirement table in which hardware requirements required for conducting a test are set for each numeric code is stored in the memory. Test requirements corresponding to the numeric code are read from the test requirement table, and a test is performed. A result of test is compared with specification evaluation values, whereby the test result is evaluated. Thus, evaluation of a test result as well as conduction of a test can be performed in the BOST device. Thus, there is no necessity of acquiring measured data into a tester. Hence, the ease of operation and convenience of the BOST device are improved, shortening of a test time becomes feasible.

Other and further objects, features and advantages of the invention will appear more fully from the following description.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a schematic diagram showing the configuration of a DSP analysis section constituting the principal feature of the first embodiment and a test method according to the first embodiment.

FIG. **2** is a signal control system diagram showing the flow of signals within a BOST board and a control system.

FIG. **3** is a schematic diagram showing the configuration of BOST control device, the flow of signals and a control system.

FIG. **4** is a schematic diagram showing the configuration of a DSP analysis section constituting the principal feature of the second embodiment and a test method according to the second embodiment.

FIG. **5** is a schematic diagram showing the configuration of a DSP analysis section constituting the principal feature of the third embodiment and a test method according to the third embodiment.

FIGS. **6**A through **6**C are schematic diagrams showing the configuration of a test apparatus for testing a semiconductor integrated circuit embodying this invention.

FIG. **7** is a block diagram showing the configuration of an electric circuit provided in the test apparatus shown in FIGS. **6**A through **6**C.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

First Embodiment

A first embodiment of the present invention will now be described by reference to a drawing.

FIGS. **6**A through **6**C are schematic diagrams showing the configuration of a test apparatus for testing a semiconductor integrated circuit embodying this invention.

FIG. **6**A is a top view of a DUT board; FIG. **6**B is a side view of the DUT board; and FIG. **6**C is a schematic diagram showing the configuration of a test machine (tester).

The test apparatus comprises a DUT board **10**; a test ancillary device (also called a BOST (built-off self-test) device)) **20**; and a tester **40**.

The DUT board **10** is designed for testing a molded IC designated by a DUT **11**. A molded IC is a semiconductor integrated circuit (IC) chip which is coated with mold resin such that a plurality of terminals are led outside from the mold resin. The IC chip mounted on the DUT **11** is, for example, a one-chip system LSI of mixed signal type. A DAC for converting a digital signal into an analog signal and an ADC for converting an analog signal into a digital signal are provided within a single chip. A hybrid integrated circuit (IC) of mixed signal type comprising a plurality of chips mounted on a common circuit board may be employed as the DUT **11**.

The DUT board **10** has a DUT socket **12** for receiving terminals of the DUT **11**. A plurality of connection terminals **13** and a cluster of relay capacitors **14** for test purposes are provided around the DUT socket **12**.

As shown in FIG. **6**B, a test head **15** is located below the DUT board **10**. The test head **15** has a plurality of connection pins **16** to be connected to the DUT board **10**. Signals required for a test are exchanged with the DUT **11** by way of the connection pins **16**.

A BOST device **20** is provided in the vicinity of the DUT board **10**. In the example of the circuit shown in FIG. **6**, the BOST device **20** is constituted on a test ancillary board (BOST board) **21**. The BOST board **21** is to be mounted on the DUT board **10**. A socket **17** is provided on the DUT board **10** for receiving the BOST board **21**. A connector **22** to be fitted to the socket **17** is provided on a lower surface of the BOST board **21**, and the connector **22** is fitted to the socket **17**. As a result, the BOST board **21** is supported on the DUT board **10**, so that signals are exchanged with the test head **15** by way of the socket **17**.

As has been known well, the BOST board **21** is an external test ancillary device (built-off self-test device) for assisting a test circuit which causes a DUT to perform a built-in self-test therein without dependence on the tester **40**. The BOST board **21** has an AD/DA measurement section **23**, a control section **24**, a DSP analysis section **25**, a memory section **26**, and a power supply section **27**.

The tester **40** has a test pattern generator (hereinafter simply called a "TPG") **41**, a power supply section **42**, and a pin electronic section **43**. The tester **40** supplies a supply voltage Vd to the BOST board **21**, thus exchanging control signals **44** with the BOST board **21**. The control signals **44** include a test analysis result signal sent from the BOST board **21** to the tester **40** as well as instruction signals sent from the tester **40** to the BOST board **21** and to the DUT board **10**.

The control signals **44**, which include a number code (a test analysis number code) and are output from the tester **40** to the BOST board **21**, are produced as test pattern signals by the TPG **41** built in the tester **40** in compliance with test signal requirements described in a test program, as in the case of a test conducted on another DUT **11**. The control signals **44** are supplied to the BOST board **21** and the DUT board **10**, by way of the pin electronic section **43** of the tester **40** having a plurality of signal I/O pins. A test analysis result (pass/fail information) output from the BOST board **21** is delivered to the pin electronic section **43** of the tester **40**. A determination section of the pin electronic section **43** acquires information about the test analysis result by comparison with a test pattern signal and through analysis of a comparison result.

FIG. **7** is a block diagram showing the configuration of an electric circuit provided in the test apparatus shown in FIGS. **6**A through **6**C.

The DUT **11** comprises an ADC **51** for converting an analog signal into a digital signal, and a DAC **52** for converting a digital signal into an analog signal.

The BOST board **21** has a testing DAC **61** for test purpose which supplies an analog test signal to the ADC **51** of the DUT **11**, and a testing ADC **62** for test purpose which converts an analog test output produced by the DAC **52** of the DUT **11** into a digital test output. Moreover, the BOST board **21** comprises a DAC input data circuit (DAC counter) **63**; a data write control circuit **64**; a measured data memory address counter **65**; measured data memory **66**; a reference clock signal circuit **67**; a clock signal generator circuit **68**; and a DSP analysis section **69**. The DSP analysis section **69** has DSP program ROM **70**.

The DAC **61**, the ADC **62**, the DAC input data circuit **63**, the data write control circuit **64**, and the measured data memory address counter **65** are included in the AD/DA measurement section **23** shown in FIGS. **6**A through **6**C. The measured data memory **66** is included in the memory section **26**, and the DSP analysis section **69** is included in the DSP analysis section **25**.

By means of such a configuration, a digital test signal (i.e., test data) is stored in the DAC input data circuit **63**. In accordance with an instruction from the tester **40**, the test data are supplied from the DAC input data circuit **63** to the DAC **52** of the DUT **11** and to the DAC **61** of the BOST board **21**.

The test data supplied to the DAC **61** are converted into an analog test signal, and the analog test signal is supplied to the ADC **51**. The ADC **51** converts the analog test signal into a digital test output, and the digital test output is supplied to the measured data memory **66**.

Meanwhile, the test data which have been supplied directly to the DAC **52** of the DUT **11** from the DAC input data circuit **63** are converted into an analog test output by the DAC **52**. The analog test output is converted into a digital test output by means of the ADC **62** of the BOST board **21**. The digital test output is supplied to the measured data memory **66**.

The measured data memory **66** sequentially stores to predetermined addresses the digital test output supplied from the ADC **51** of the DUT **11**, and the digital test output supplied from the DAC **52** by way of the ADC **62**.

The ADC **51** of the DUT **11** and the ADC **62** of the BOST board **21** convert an analog signal into a digital signal, sequentially. Every time a single digital signal is output, the ADC **51** and the ADC **62** each output a BUSY signal. The BUSY signals are supplied to the data write control circuit **64** provided on the BOST board **21**. On the basis of the thus-supplied BUSY signals, the data write control circuit **64** sequentially advances the digital test data pertaining to the DAC input data circuit **63** to the next digital test data on a per-data-set basis. Further, the data write control circuit **64** acts on the measured data memory address counter **65** so as to sequentially advance an address of the measured data memory **66**.

As mentioned above, a code of the digital test data to be converted by the DUT **11** is advanced by the DAC input data circuit **63**. As a result of sequential advancement of an address on the measured data memory **66** at which the digital test output converted by the DUT **11** is to be stored, the ADC **51** and the DAC **52** provided in the DUT **11** sequentially pursue conversion required by a test. The thus-converted measured data are sequentially stored in the measured data memory **66**. In subsequent processes, conversion tests proceed until a final code set by the DSP analysis section **69** on the BOST board **21** is achieved, and the results of all conversion tests are stored in the measured data memory **66**.

After the ADC **51** and the DAC **52** of the DUT **11** have completed conversion tests, the DSP analysis section **69** provided on the BOST board **21** sequentially reads conversion data stored in the measured data memory **66**, through use of a program stored in the DPG program ROM **70**, thus analyzing a conversion characteristic. The analysis includes computation of an A/D conversion characteristic parameter, a D/A conversion characteristic parameter, a differential linearity, and an integral nonlinearity error. An analysis result (pass/fail information) is sent from the BOST board **21** to the tester **40**, wherein the tester **40** processes a test result.

In the configuration shown in FIGS. **6**A through **6**C, the BOST board **21** is provided in the vicinity of the DUT board **10** and has the function of causing the ADC **51** and DAC **52** of the DUT **11** to perform conversion tests. The conversion tests can be effected on the BOST board **21**.

Consequently, an analog measurement system line provided between the DUT board **10** and the BOST board **21** can be shortened, and occurrence of a measurement error attributable to noise can be suppressed sufficiently. Thus, a high-precision test can be implemented, and a test can be carried out at a higher speed on the basis of a signal exchanged between the DUT board **10** and the BOST board **21** located in the vicinity thereof.

An analog measurement system line can be obviated from an area between the BOST board **21** and the tester **40**, thereby increasing the accuracy of a test. After required conversion tests have been completed on the BOST board **21**, the results of conversion tests are sent to the tester **40**. Thus, a test speed can be increased as compared with a case in which converted data are transmitted to the tester **40**.

In the apparatus shown in FIGS. **6**A through **6**C, the conversion test function of the ADC **51** and that of the DAC **52** of the DUT **11** are implemented on the BOST board **21**. Hence, there is no necessity of adding a powerful conversion test function to the tester **40**. Hence, an increase in the cost of the tester **40** is prevented, thereby enabling diversion of a conventional low-speed tester to the test apparatus. When a tester **40** having a special measurement function is to be manufactured, limitations are imposed on expansion of capabilities of hardware configuration of a tester. Further, manufacture of such a tester **40** involves modifications to the tester itself, posing a fear of a hike in development costs.

The test apparatus shown in FIGS. **6**A through **6**C utilizes as standard equipment a TPG and pin electronics provided on a common tester. Configuration and control of a BOST board can be effected without being influenced by specifications of testers or restrictions. Thus, application of the test apparatus to various types of testers is feasible.

FIG. **1** is a schematic diagram showing the configuration of a DSP analysis section constituting the principal feature of the first embodiment and a test method according to the first embodiment. The test apparatus shown in FIG. **1** is identical in configuration with that shown in FIGS. **6** and **7**, exclusive of the DSP analysis section. Hence, these drawings are employed, and repeated explanation of the test apparatus is omitted.

In the present embodiment, numeric codes are assigned to tests on DUTs **11** to be performed by a BOST device **20**. Requirements settings—which are required for a test and are to be made on hardware of the BOST device **20**—are registered on a test requirement table **71** in FIG. **1** for each numeric code. The test requirement table **71** is stored in memory (not shown) integrated in a processor of a DSP analysis section **69** provided on the BOST device **20** or in memory (not shown) provided on a BOST device connected to the DUTs **11**. When the numeric code (i.e., a test analysis number) is transmitted to the BOST device **20** from an external controller or the tester **40**, the processor reads corresponding setting requirements from the test requirement table **71**. The thus-read setting requirements are set in the hardware of the BOST device **20**, whereupon a test is commenced.

Software processing to be performed in the processor of the DSP analysis section **69** will next be described. As shown in FIG. **1**,

(1) the numeric code assigned to a test (i.e., a test analysis number) which has been entered into the processor is inputted to the inside of the processor in step S1.

(2) Test requirements corresponding to the test analysis number that has been inputted are read from the test requirement table **71** in step S2.

(3) In step S3, the thus-read test requirements are set in a BOST hardware function block **72** provided outside the processor.

(4) Processing pertaining to (3) is iterated until all the requirement setting are completed.

Next will be described a circuit for performing a round of operations from entry of the test analysis number to setting of requirements on hardware of the BOST device **20** as well as the operation of the circuit.

FIG. **2** is a signal control system diagram showing the flow of signals within a BOST board **21** and a control system. The series of processing operations are performed by the DSP analysis section **69** and a BOST control circuit **75** whose detailed circuit is shown in FIG. **3**.

Operations of circuits shown in FIGS. **2** and **3** will be described.

(1) A frame signal (B-SFRAM), a data signal (B-SDATA), and a clock signal (B-SCLK) are inputted to a BOST control circuit **75** from an external controller, such as a TPG **41** of the tester **40**. In connection with these signals, the frame signal is taken as an input start signal, and the data signal is serially inputted to the BOST device **20** in synchronism with the clock signal. The data signal following the frame signal in the next cycle is a mode M signal. When the mode M signal assumes a value of 0, the value means that the following serial data represent a test analysis number. When the mode M signal assumes a value of 1, the value means that the following serial data represent an IP address (identification address) assigned to each block of the hardware of the BOST device **20** and setting data to be written into the address or read from the address. When the signals are inputted from the external controller, such as a tester, to the BOST device **20**, a mode R/W signal following the mode M signal in the next cycle assumes a value of 0. In contrast, when the signals are inputted from the BOST **20** to the external controller, such as a tester, the mode R/W signal assumes a value of 1. In short, the mode R/W signal shows the direction of the serial data signal.

(2) When the test analysis number is inputted to the BOST device **20**, a first mode M register **77** and a first mode R/W register **78** are reset by a frame signal by a serial data I/O switching section **76** shown in FIG. **3**. At this time, a serial data I/O port is switched to the direction in which a signal is output from the external controller to the BOST device **20**. Subsequently, mode information is set in the first mode M register **77** and the first mode R/W register **78**. (3) Since the first mode M register **77** latches 0, a first switching circuit MUX1 of the serial data I/O switching section **76** causes the frame signal, the data signal, and the clock signal, which have been inputted to the BOST device **20**, to enter a serial port **0** of the DSP analysis section **69**, where the signals are subjected to software processing shown in FIG. **1**.

(4) Requirements are set in the hardware of the BOST device **20** by the DSP analysis section **69**, by the frame signal, the data signal, and the clock signal appearing at a serial port **1** of the DSP analysis section **69**. The signals are inputted to the BOST control circuit **75**. A serial-to-parallel conversion section **79B** of a RD/WR control section **79** converts a device address signal and a data signal into parallel signals and retains the thus-converted parallel signals.

Since a second mode M register **80** and a second mode R/W register **81** assume a value of 0 after conversion, a read/write signal generation section **79C** produces a write signal. The write signal is inputted to corresponding hardware along with the data signal, by way of a H/W write signal line assigned a corresponding device address signal by a third switching circuit MUX **3** which takes, as a switching signal, the device address signal that have been converted into a parallel signal. Data are retained by the write signal.

As in the case of the first mode M register **77**, a second mode M register **80** selects a DSP analysis section when latching a value of 0 and signal groups output from the external controller when latching a value of 1. A second mode R/W register **81** operates in the same manner as the first mode R/W register **78**.

(5) Meanwhile, when written data are verified by the DSP analysis section **69**, processing identical with that mentioned previously is performed through use of the frame signal, the data signal, and the clock signal output from the serial port **1** of the DSP analysis section **69** as well as through use of the frame signal, the data signal, and the clock signal input to the serial port **1** of the DSP analysis section **69**. At this time, on the basis of the information set on the second mode M register **80** and the second mode R/W register **81**, the write/read signal generation section **79C** produces a read signal. The read signal is taken as a reference signal to be used for producing a frame signal and a clock signal when H/W setting data are sent to the serial port **1** of the DSP analysis section **69**. Reading operation of the DSP analysis section is as follows. Namely, in accordance with the device address signal retained by the serial-to-parallel conversion section **79B** of the device address RD/WR control section **79**, a fourth switching circuit MUX **4** selects corresponding H/W output data. A parallel-to-serial conversion section **79A** of the RD/WR control section **79** converts the data into serial data, and the thus-converted serial data are inputted to the serial port **1** of the DSP analysis section **69**. The DSP analysis section **69** receives the data and verifies the data through software processing. As mentioned previously, the read signal output from the read/write signal generation section **79** and a DSP-compatible conversion clock signal produced from the read signal by a clock signal generation section of the parallel-to-serial conversion section **79A** are used as the frame signal and the clock signal used in entering data into the serial port **1**.

The operations which have been described thus far correspond to the series of operations from entry of a test analysis number to setting of hardware requirements on the BOST device **20**. In addition, setting data on the hardware of the BOST device **20** from the external controller and reading the setting data from the same can be effected for the purpose of verifying circuits of the BOST device **20**. This can be effected when the mode M signal assumes a value of 1. In connection with writing of data, processing pertaining to (4) is performed through use of the signals output from the external controller rather than the signals output from the serial port **1** of the DSP analysis section **69**. In connection with reading of data, data are inputted from the external controller in synchronism with the clock signal which is output from the external controller and is taken as a conversion clock signal of the parallel-to-serial conversion section **79A** of the RD/WR control section **79** employed in the processing pertaining to (5).

The circuit configuration is controlled by a serial signal. Hence, the number of pins to be provided on a tester can be diminished as compared with a case where a circuit is controlled by the TPG **41** of the tester. As a result, limitations imposed on an increase in the number of DUTs **11** which can be measured simultaneously can be alleviated.

Since the circuit according to the first embodiment is configured in the manner as mentioned above, the processor of the DSP analysis section **69** of the BOST device **20** can

download test requirements directly to individual sections of the BOST device **20** by transmission of only a test analysis number. Setting information to be output from the external controller is simplified, thus improving the ease of operation and convenience of the BOST device.

Further, as in the case of an analysis program, requirements for setting hardware of the BOST device **20** can be collectively managed by ROM of the processor provided in the DSP analysis section **69**.

Further, there can be curtailed an excessive communications time, which would otherwise be caused when requirements are set from the outside of the BOST device **20**, there by speeding up setting operation. Further, there is yielded an advantage of shortening of a test time.

Second Embodiment

A second embodiment of the present invention will now be described by reference to a drawing.

FIG. **4** is a schematic diagram showing the configuration of a DSP analysis section constituting the principal feature of the second embodiment and a test method according to the second embodiment. The test apparatus shown in FIG. **4** is identical in configuration with that shown in FIGS. **6** and **7**, exclusive of the DSP analysis section. Hence, these drawings are employed, and repeated explanation of the test apparatus is omitted.

As in the case of the first embodiment, in the present embodiment tests on the DUTs **11** to be performed by the BOST device **20** are converted into numeric codes. A test analysis table **85** has a memory address table **82** for setting an address of measured data memory in which measured data are stored on a per-numeric-code basis; a computation method table **83** in which computation method information required for conducting the tests is arranged in the form of a table for on a per-numeric-code basis; and a test specification table **84** in which specification evaluation values are arranged in the form of a table. The test analysis table **85** is stored in memory integrated in the processor of the DSP analysis section **69** provided on the BOST device **20** or in memory provided on a BOST device connected to the DUTs **11**. When a test analysis number is transmitted to the BOST device **20** from the tester or the external controller and when an analysis start signal is inputted to the processor, the processor reads measured data from the measured data memory **66**, thereby evaluating specifications. Test information result (pass/fail) is transmitted to the external controller.

Software processing to be performed in the processor of the DSP analysis section **69** will next be described. As shown in FIG. **4**,

(1) the numeric code assigned to a test (i.e., a test analysis number) which as been entered into the processor of the DSP analysis section **69** is inputted to the inside of the processor in step S1.

(2) An address on the measured data memory—in which are stored measured data corresponding to the test analysis number that has been inputted—is read from a memory address table **82** in step S12, and the thus-read address is set.

(3) In step S13 corresponding measured data are read from the measured data memory **66** on the basis of the memory address, and the thus-read measured data are inputted to the processor.

(4) A computation technique corresponding to the test analysis number that has been inputted is read from a computation technique table **83** in step S14.

(5) In step S15, ADC characteristic parameters and DAC characteristic parameters (i.e., a differential linearity and an integral nonlinearity error) of the DUTs **11** are computed from the measured data and by means of the computation technique.

(6) In step S16, a specification evaluation value corresponding to the test analysis number that has been inputted is read from the test specification table **84**. The specification evaluation value is compared with a result of computation performed in step S15, thus effecting pass/fail evaluation.

(7) In step S17, a result of the test performed in step S16 is sent to the external controller.

Transmission of the test result will now be described.

When a test result is transmitted, information about the test result (also called "test result information") is latched in an error code register **86** by means of a frame signal, a data signal (representing test result information), and a clock signal, which are output from the serial port **0** of the DSP analysis section **69** shown in FIG. **3**. In connection with reading of the information, the frame signal, the data signal, and the clock signal, which are output from the external controller, are inputted to the BOST device **20**, wherein the data signal has imparted a value of "0" to mode M information and a value of "1" to mode R/W information. A second switching circuit MUX **2** selects an output from the error code register **86** and transmits the test result information to the external controller in synchronism with the clock signal.

Since the DSP analysis section according to the second embodiment is configured in the manner as mentioned above, the BOST device **20** effects pass/fail evaluation of an ordinary test. There is no necessity of transmitting and loading measured data to the tester, thereby improving the ease of operation and convenience of the BOST device.

As a result of simplification of a test result, an effect of shortening a test time can be expected.

Third Embodiment

A third embodiment of the present invention will now be described by reference to a drawing.

FIG. **5** is a schematic diagram showing the configuration of a DSP analysis section constituting the principal feature of the third embodiment and a test method according to the third embodiment. The test apparatus shown in FIG. **5** is identical in configuration with that shown in FIGS. **6** and **7**, exclusive of the DSP analysis section. Hence, these drawings are employed, and repeated explanation of the test apparatus is omitted.

As shown in FIG. **5**, in the present embodiment, a measured data transmission method table **86** in which transmission methods for outputting measured data are stored is provided in the test analysis table **85**. When there is transmitted a test analysis number corresponding to the table number stored in which the transmission method is stored, the processor of the DSP analysis section **69** provided on the BOST device **20** reads corresponding measured data from the measured data memory **66**. The thus-read measured data are transmitted to the external controller.

Software processing to be performed in the processor of the DSP analysis section **69** will next be described.

As shown in FIG. **5**,

(1) The test analysis number input to the processor of the DSP analysis section **69** is inputted to the processor in step S21.

(2) For example, in a case where the most significant bit of the test analysis number is "0", the test analysis number is perceived as representing measured data processing. First, in step S22 a measured data output method corresponding to the test analysis number is read from the measured data transmission method table **86**.

The measured data transmission method corresponds to software processing to be performed for outputting measured data to the outside.

(3) In step S23, an address on the measured data memory 66 in which are stored measured data corresponding to the test analysis number which has been inputted is read from the memory address table 82, and the thus-read address is set.

(4) In step S24, corresponding measured data are loaded from the memory address and into the processor of the DSP analysis section 69.

(5) In step S25, the measured data are transmitted to the outside.

Since the DSP analysis section according to the third embodiment is configured in the manner as mentioned above, measured data can be readily loaded from the outside. The measured data can be processed and cataloged outside of the DSP analysis section by means of software. The DSP analysis section can be used for conducting a normal test but also for evaluating and analyzing design of a DUT.

Obviously many modifications and variations of the present invention are possible in the light of the above teachings. It is therefore to be understood that within the scope of the appended claims the invention may by practiced otherwise than as specifically described.

The entire disclosure of a Japanese Patent Application No. 2001-32847, filed on Feb. 8, 2001 including specification, claims, drawings and summary, on which the Convention priority of the present application is based, are incorporated herein by reference in its entirety.

What is claimed is:

1. An apparatus for testing a semiconductor integrated circuit comprising:

a test circuit board configured to transmit signals to and receive signals from a semiconductor integrated circuit to be tested, wherein the semiconductor integrated circuit comprises an A/D converter circuit to convert analog signals to digital signals and a D/A converter circuit to convert digital signals to analog signals;

a test ancillary device which is disposed in the vicinity of said test circuit board and is connected to said test circuit board; and

an external controller which assigns a numeric codes to tests to be conducted on said semiconductor integrated circuit by said test ancillary device and which transmits said numeric codes to said test ancillary device, wherein said test ancillary device comprises:

memory having stored therein a test requirement table in which hardware requirements required for conducting the tests, which are applied to the test ancillary device, are set for each corresponding numeric code;

an analysis section for reading test requirements corresponding to one of said numeric codes from said test requirement table;

a data circuit for supplying a digital test signal to said D/A converter circuit of said semiconductor integrated circuit to be tested on the basis of said test requirements read by said analysis section;

a testing D/A converter circuit which converts the digital test signal from said data circuit into an analog test signal and supplies said analog test signal to said A/D converter circuit of said semiconductor integrated circuit to be tested;

a testing A/D converter circuit which converts an analog test output from said D/A converter circuit of said semiconductor integrated circuit to be tested into a digital test output; and

measured data memory for storing the digital test output from said A/D converter circuit of said semiconductor integrated circuit to be tested and said digital test output from said testing A/D converter circuit,

wherein a result of analysis of said each digital test outputs stored in said measured data memory, the analysis being performed by said analysis section, is sent to said external controller.

2. The apparatus for testing a semiconductor integrated circuit according to claim 1, wherein said external controller is a tester.

3. The apparatus for testing a semiconductor integrated circuit according to claim 1, wherein said memory having stored therein said test requirement table is incorporated in said analysis section.

4. The apparatus for testing a semiconductor integrated circuit according to claim 1, wherein said test ancillary device comprises:

a test analysis table having a memory address table for setting an address of the measured data memory in which digital test outputs are stored for a corresponding numeric code;

a computation method table having stored therein information about computation methods corresponding to respective numeric codes; and

a test specification table in which specification evaluation values corresponding to the respective numeric codes are stored, wherein

when an analysis start instruction is received from said external controller along with a numeric code, a predetermined digital test output is read from said memory address table; a corresponding computation method is read from the computation method table, thereby computing a characteristic parameter of said A/D converter circuit of said semiconductor integrated circuit to be tested and a characteristic parameter of said D/A converter circuit of the same; a result of computation is compared with a specification evaluation value corresponding to the numeric code read from said test specification table, thus evaluating a specification; and a result of evaluation is sent to said external controller.

5. The apparatus for testing a semiconductor integrated circuit according to claim 4, wherein said characteristic parameters correspond to a differential linearity and an integral nonlinearity error.

6. The apparatus for testing a semiconductor integrated circuit according to claim 4, wherein transmission information for sending a digital test output is provided in said test analysis table; and, when a numeric code corresponding to transmission information is sent to said test ancillary device from said external controller, said test ancillary device reads a corresponding digital test output from said measured data memory, and the digital test output is sent to said external controller.

7. The apparatus for testing a semiconductor integrated circuit according to claim 6, wherein the numeric code to be used for selecting transmission information is formed by combination of a code representing details of a test and a code to be used for selecting transmission information.

8. A method for testing a semiconductor integrated circuit comprising, a test circuit board configured to transmit signals to and receive signals from a semiconductor integrated circuit to be tested wherein the semiconductor integrated circuit comprises an A/D converter circuit to convert analog signals to digital signals and a D/A converter circuit to

convert digital signals to analog signals, the methods comprising the steps of:

assigning a numeric code to each one of a test requirement stored in a test requirement table for tabulating hardware requirements for conducting test on said semiconductor integrated circuit to be tested;

reading a test requirement corresponding to one of said numeric codes from said test requirement table;

outputting a digital test signal on the basis of said test requirement read;

outputting the digital test signal to said D/A converter circuit of said semiconductor integrated circuit;

converting the digital test signal into an analog test signal and outputting the analog signal to said A/D converter circuit of said semiconductor integrated circuit;

converting an analog signal output from said D/A converter circuit to a first digital test output;

storing the first digital test output and storing a second digital test output from from said A/D converter circuit of said semiconductor integrated circuit;

conducting an analysis of the first digital test output and the second digital test output, and outputting a result of the analysis.

* * * * *

US006331770B1

(12) **United States Patent**
Sugamori

(10) **Patent No.: US 6,331,770 B1**
(45) **Date of Patent: Dec. 18, 2001**

(54) **APPLICATION SPECIFIC EVENT BASED SEMICONDUCTOR TEST SYSTEM**

(75) Inventor: **Shigeru Sugamori**, Santa Clara, CA (US)

(73) Assignee: **Advantest Corp.**, Tokyo (JP)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **09/547,753**

(22) Filed: **Apr. 12, 2000**

(51) **Int. Cl.**[7] **G01R 7/00**
(52) **U.S. Cl.** **324/158.1**; 324/760; 341/120; 714/724
(58) **Field of Search** 324/158.1, 765, 324/760; 341/120; 371/22.3; 714/724–737

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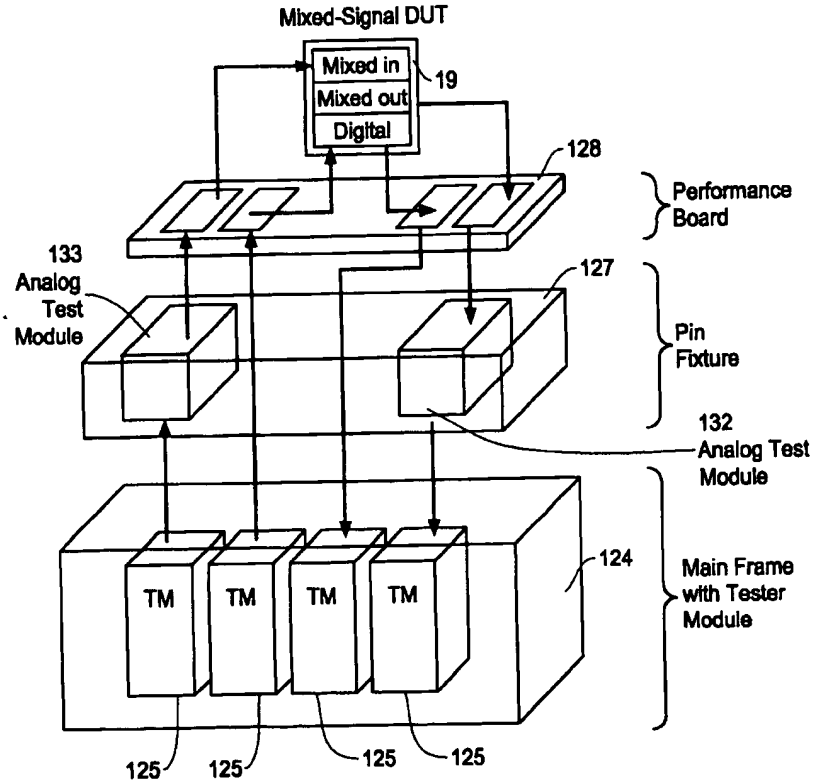
Primary Examiner—Safet Metjahic
Assistant Examiner—Jimmy Nguyen
(74) *Attorney, Agent, or Firm*—Muramatsu & Associates

(57) **ABSTRACT**

A semiconductor test system for testing semiconductor devices, and particularly, to a semiconductor test system having a plurality of different types of tester modules in a main frame and a measurement module unique to the device under test in a test fixture, thereby achieving a low cost and application specific test system. The semiconductor test system includes two or more tester modules whose performances are different from one another, a test system main frame to accommodate a combination of two or more tester modules, a test fixture provided on the main frame for electrically connecting the tester modules and a device under test, a measurement module provided in the test fixture for converting signals between the device under test and the tester module depending on the function of the device under test, and a host computer for controlling an overall operation of the test system by communicating with the tester modules through a tester bus.

12 Claims, 10 Drawing Sheets



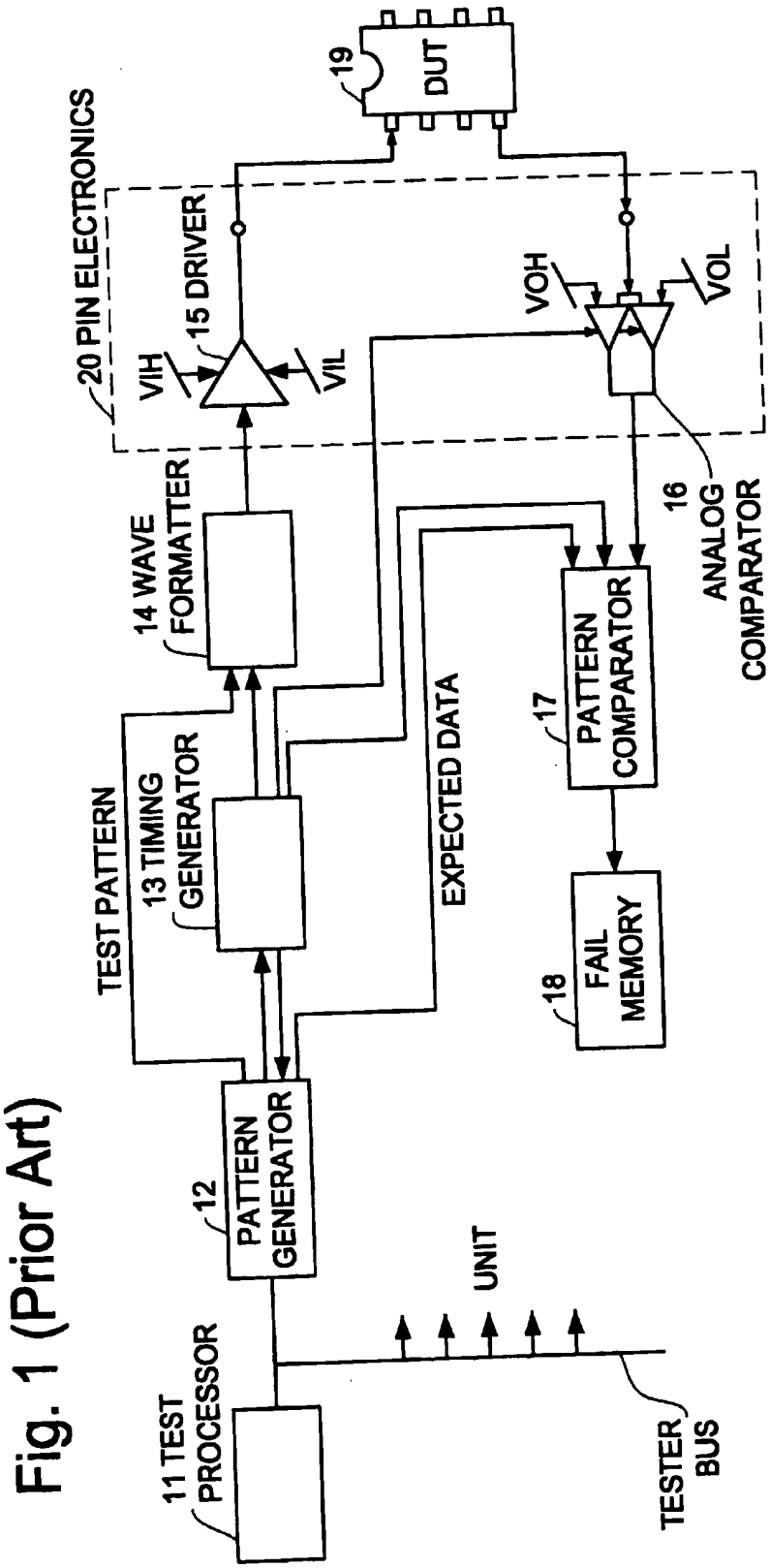
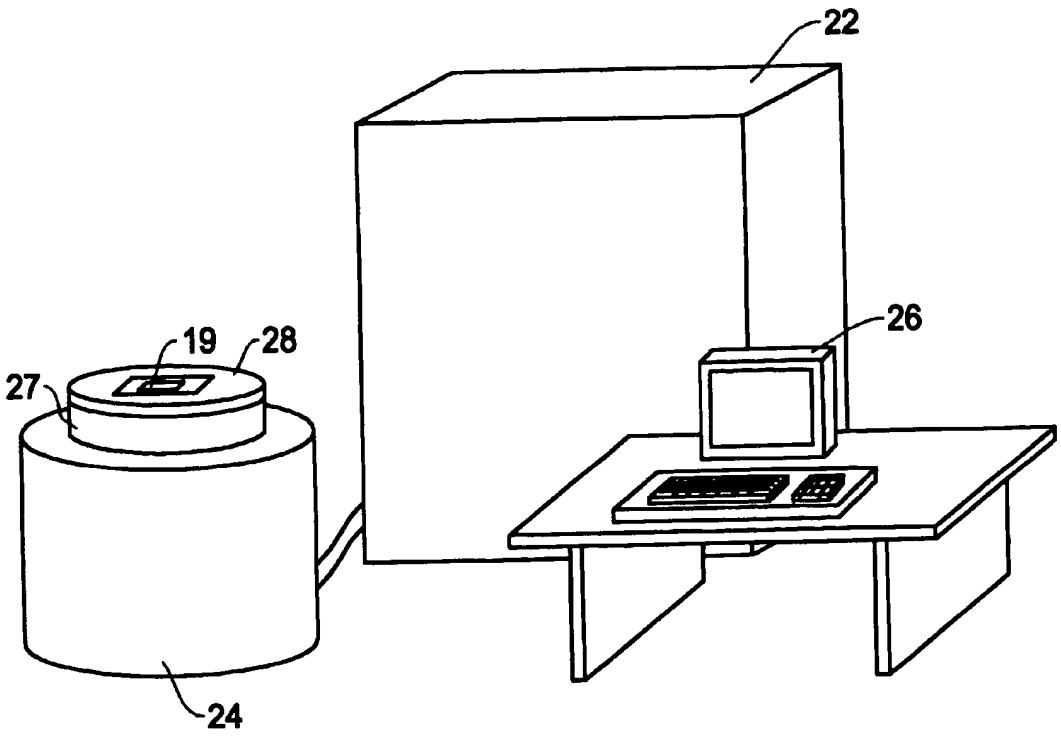


Fig. 1 (Prior Art)

Fig. 2 (Prior Art)



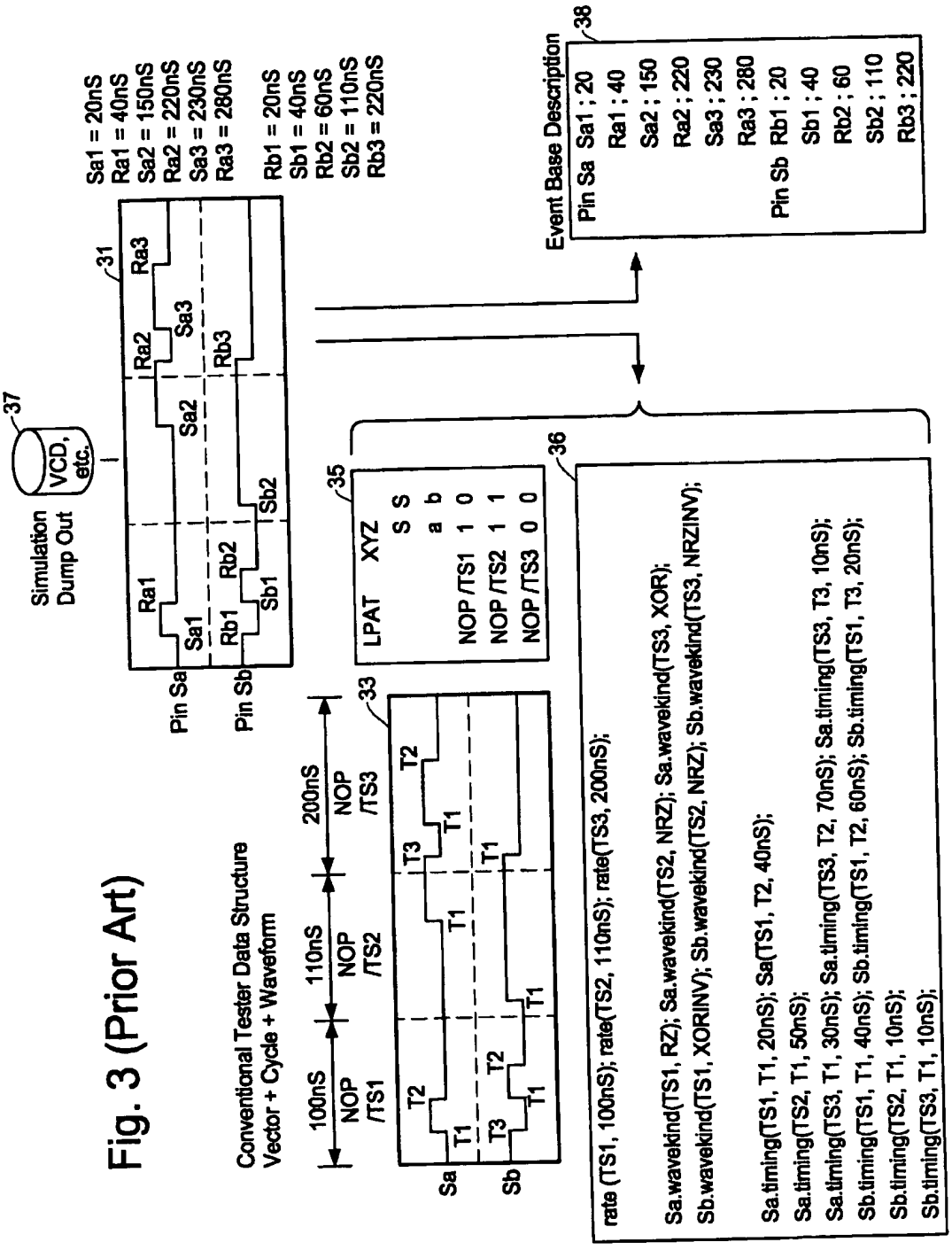


Fig. 3 (Prior Art)
Simulation Dump Out
VCD, etc.
37
31
Pin Sa
Pin Sb
Sa1 = 20nS
Ra1 = 40nS
Sa2 = 150nS
Ra2 = 220nS
Sa3 = 230nS
Ra3 = 280nS
Rb1 = 20nS
Sb1 = 40nS
Rb2 = 60nS
Sb2 = 110nS
Rb3 = 220nS
Conventional Tester Data Structure
Vector + Cycle + Waveform
100nS NOP /TS1
110nS NOP /TS2
200nS NOP /TS3
33
Sa
Sb
LPAT XYZ
S S
a b
NOP /TS1 1 0
NOP /TS2 1 1
NOP /TS3 0 0
35
Event Base Description
38
Pin Sa Sa1 ; 20
Ra1 ; 40
Sa2 ; 150
Ra2 ; 220
Sa3 ; 230
Ra3 ; 280
Pin Sb Rb1 ; 20
Sb1 ; 40
Rb2 ; 60
Sb2 ; 110
Rb3 ; 220
36
rate (TS1, 100nS); rate(TS2, 110nS); rate(TS3, 200nS);
Sa.wavekind(TS1, RZ); Sa.wavekind(TS2, NRZ); Sa.wavekind(TS3, XOR);
Sb.wavekind(TS1, XORINV); Sb.wavekind(TS2, NRZ); Sb.wavekind(TS3, NRZINV);
Sa.timing(TS1, T1, 20nS); Sa(TS1, T2, 40nS);
Sa.timing(TS2, T1, 50nS);
Sa.timing(TS3, T1, 30nS); Sa.timing(TS3, T2, 70nS); Sa.timing(TS3, T3, 10nS);
Sb.timing(TS1, T1, 40nS); Sb.timing(TS1, T2, 60nS); Sb.timing(TS1, T3, 20nS);
Sb.timing(TS2, T1, 10nS);
Sb.timing(TS3, T1, 10nS);

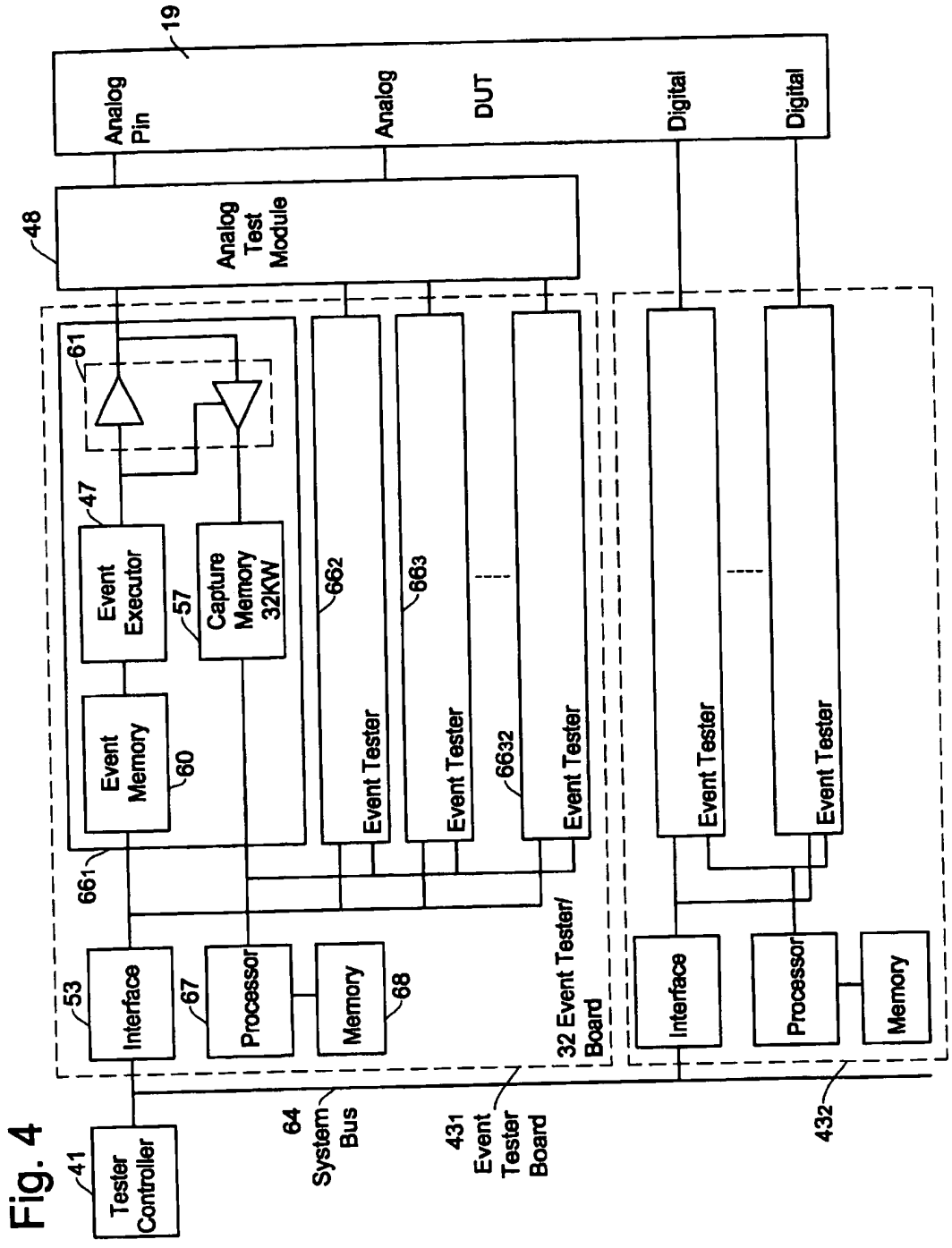

19
Analog Pin
Analog
DUT
Digital
Digital
48
Analog Test Module
61
47
Event Executor
57
Capture Memory 32KW
662
663
6632
Event Tester
Event Tester
Event Tester
Event Tester
Event Tester
Event Memory
60
661
53
Interface
67
Processor
Memory
68
32 Event Tester/ Board
Interface
Processor
Memory
64
System Bus
431
Event Tester Board
432
41
Tester Controller

Fig. 4

Fig. 5

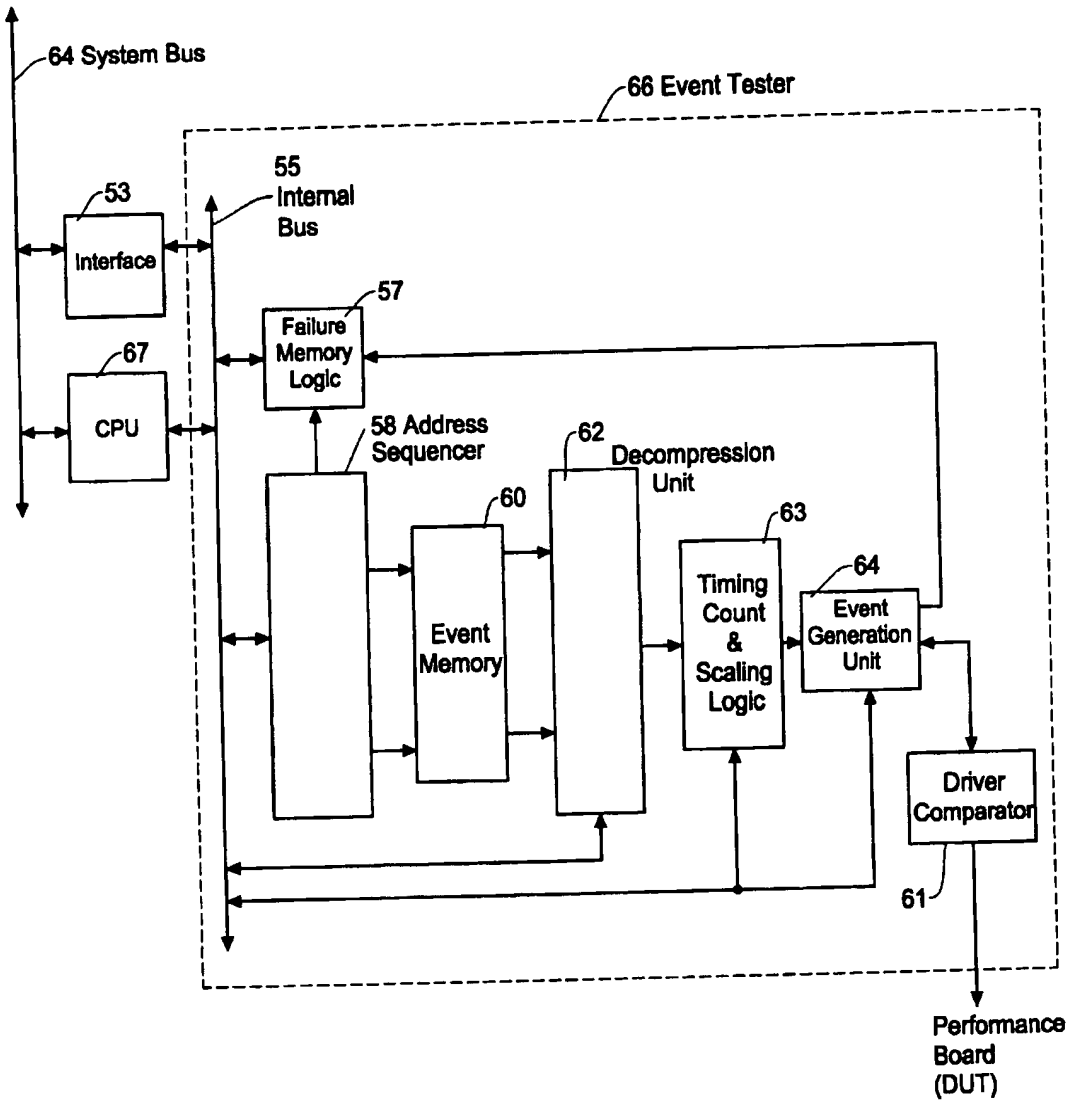

64 System Bus
66 Event Tester
55
Internal
Bus
53
Interface
57
Failure
Memory
Logic
67
CPU
58 Address
Sequencer
62
Decompression
Unit
60
Event
Memory
63
Timing
Count
&
Scaling
Logic
64
Event
Generation
Unit
Driver
Comparator
61
Performance
Board
(DUT)

Fig. 6

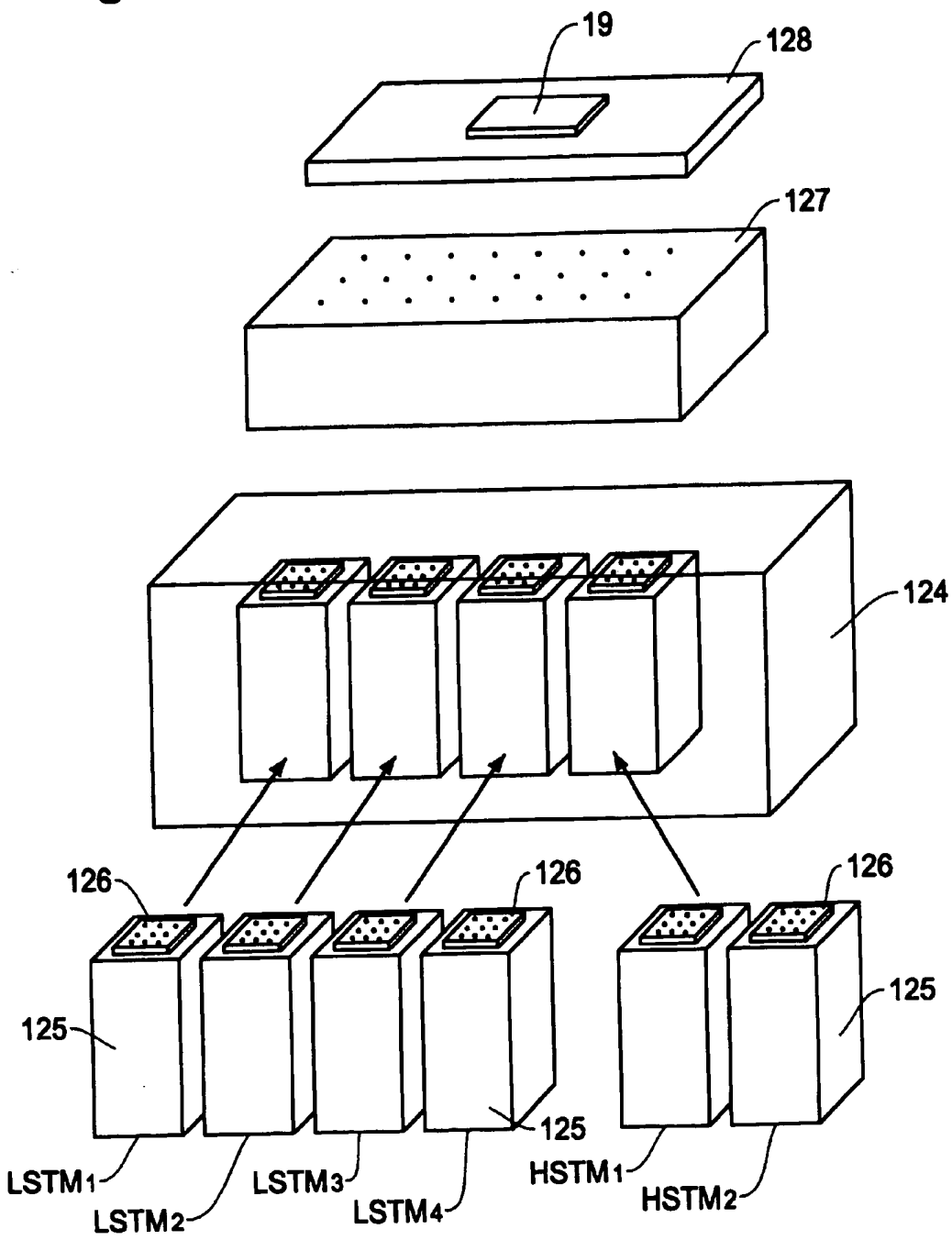

19
128
127
124
126
126
126
125
125
125
LSTM1
LSTM2
LSTM3
LSTM4
HSTM1
HSTM2

Fig. 7A

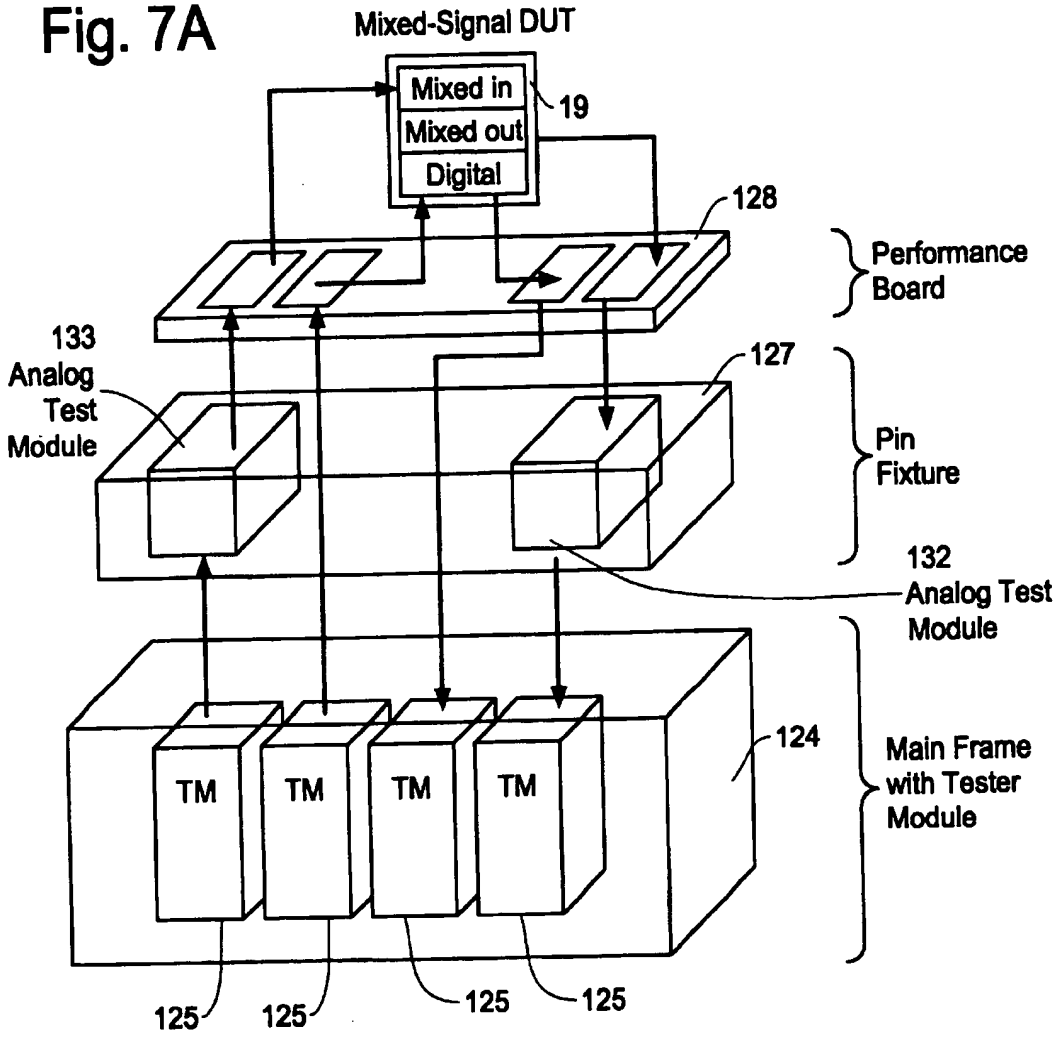

Mixed-Signal DUT
Mixed in
Mixed out
Digital
19
128
Performance Board
133
Analog Test Module
127
Pin Fixture
132
Analog Test Module
124
TM
TM
TM
TM
Main Frame with Tester Module
125
125
125
125

Fig. 7B

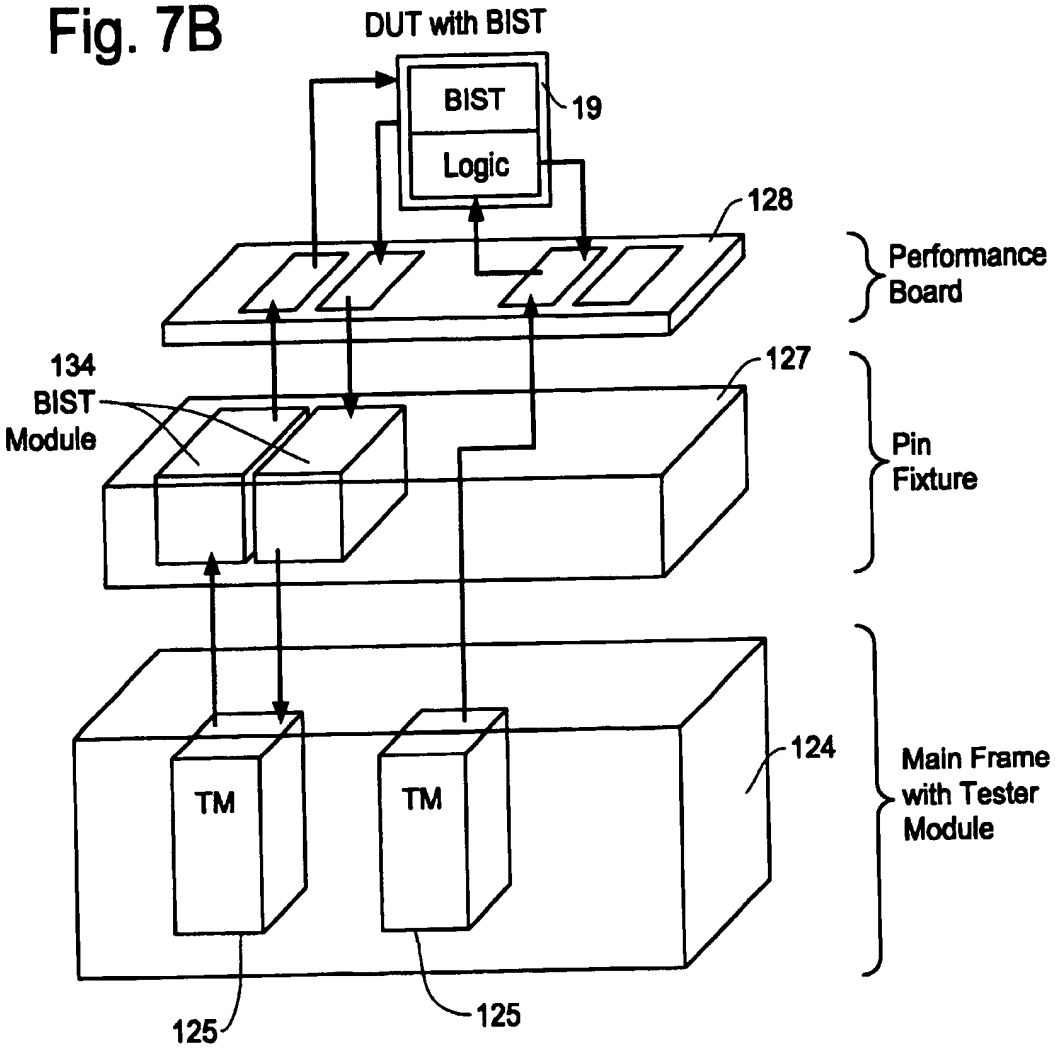

DUT with BIST
BIST
Logic
19
128
Performance Board
134
BIST Module
127
Pin Fixture
TM
TM
124
Main Frame with Tester Module
125
125

Fig. 8

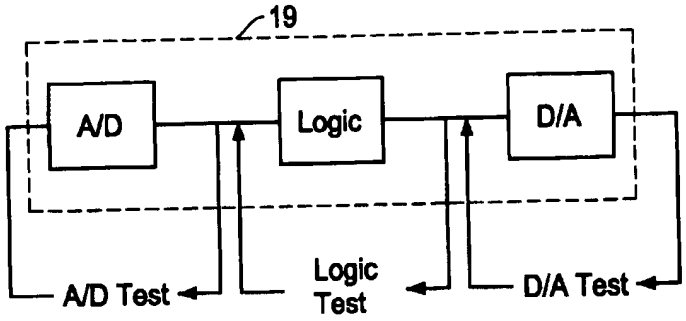


Fig. 9A

Fig. 9B

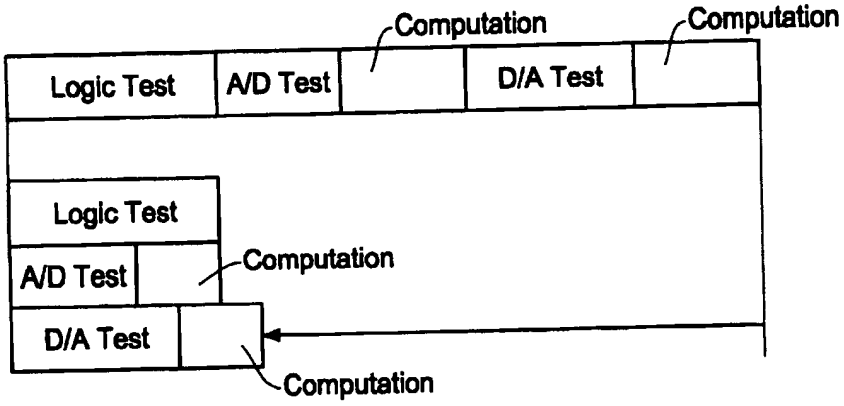
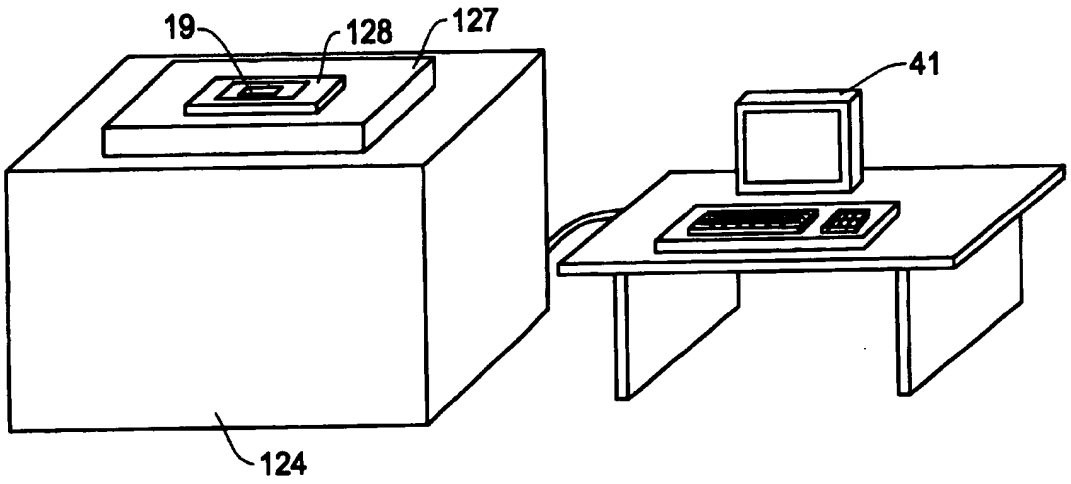


Fig. 10



APPLICATION SPECIFIC EVENT BASED SEMICONDUCTOR TEST SYSTEM

FIELD OF THE INVENTION

This invention relates to a semiconductor test system for testing semiconductor integrated circuits such as a large scale integrated (LSI) circuit, and more particularly, to a low cost semiconductor test system configured exclusively to a specific application and has an event based tester architecture. The event based semiconductor test system of the present invention is formed by freely combining a plurality of tester modules having identical or different capabilities and a measurement module specific to an intended application where each of the tester module operates independently from one another, thereby establishing a low cost test system. The measurement module may be installed in a test fixture of the test system.

BACKGROUND OF THE INVENTION

FIG. **1** is a schematic block diagram showing an example of a semiconductor test system, also called an IC tester, in the conventional technology for testing a semiconductor integrated circuit (hereafter may also be referred to as "device under test").

In the example of FIG. **1**, a test processor **11** is a dedicated processor provided within the semiconductor test system for controlling the operation of the test system through a tester bus. Based on pattern data from the test processor **11**, a pattern generator **12** provides timing data and waveform data to a timing generator **13** and a wave formatter **14**, respectively. A test pattern is produced by the wave formatter **14** with use of the waveform data from the pattern generator **12** and the timing data from the timing generator **13**, and the test pattern is supplied to a device under test (DUT) **19** through a driver **15**.

A response output signal from the DUT **19** is produced in response to the test pattern. The output signal is converted to a logic signal by an analog comparator **16** with reference to a predetermined threshold voltage level. The logic signal is compared with expected value data from the pattern generator **12** by a logic comparator **17**. The result of the logic comparison is stored in a failure memory **18** corresponding to the address of the DUT **19**. The driver **15**, the analog comparator **16** and switches (not shown) for changing pins of the device under test, are provided in a pin electronics **20**.

The circuit configuration noted above is provided to each test pin of the semiconductor test system. Therefore, since a large scale semiconductor test system has a large number of test pins, such as from 256 test pins to 1048 test pins, and the same number of circuit configurations each being shown in Figure are incorporated, an actual semiconductor test system becomes a very large system. FIG. **2** shows an example of outer appearance of such a semiconductor test system. The semiconductor test system is basically formed with a main frame **22**, a test head **24**, and a work station **26**.

The work station **26** is a computer provided with, for example, a graphic user interface (GUI) to function as an interface between the test system and a user. Operations of the test system, creation of test programs, and execution of the test programs are conducted through the work station **26**. The main frame **22** includes a large number of test pins each having the test processor **11**, pattern generator **12**, timing generator **13**, wave formatter **14** and comparator **17** shown in FIG. **1**.

The test head **24** includes a large number of printed circuit boards each having the pin electronics **20** shown in FIG. **1**.

The test head **24** has, for example, a cylindrical shape in which the printed circuit boards forming the pin electronics are radially aligned. On an upper surface of the test head **24**, a device under test **19** is inserted in a test socket at about the center of a performance board **28**.

Between the pin electronics circuit and the performance board **28**, a pin (test) fixture **27** is provided which is a contact mechanism for communication of electrical signals. The pin fixture **27** includes a large number of contractors such as pogo-pins for electrically connecting the pin electronics circuits and the performance board. The device under test **19** receives a test pattern signal from the pin electronics and produces a response output signal.

In the conventional semiconductor test system, for producing a test pattern to be applied to a device under test, the test data which is described by, what is called a cycle based format, has been used. In the cycle based format, each variable in the test pattern is defined relative to each test cycle (tester rate) of the semiconductor test system. More specifically, test cycle (tester rate) descriptions, waveform (kinds of waveform, edge timings) descriptions, and vector descriptions in the test data specify the test pattern in a particular test cycle.

In the design stage of the device under test, under a computer aided design (CAD) environment, the resultant design data is evaluated by using a logic simulation process through a test bench. However, the design evaluation data thus obtained through the test bench is described in an event based format. In the event based format, each change point (event) in the particular test pattern, such as from "**0**" to "1" or from "1", to "0", is described with reference to a time passage. The time passage is expressed by, for example, an absolute time length from a predetermined reference point or a relative time length between two adjacent events.

The inventors of this invention has disclosed the comparison between the test pattern formation using the test data in the cycle based format and the test pattern formation using the test data in the event based format in the U.S. patent application Ser. No. 09/340,371. The inventors of this invention have also proposed an event based test system as a semiconductor test system as a new concept test system. The details of the structure and operation of the event based test system is given in the U.S. patent application Ser. No. 09/406,300 owned by the same assignee of this invention.

As described in the foregoing, in the semiconductor test system, a large number of printed circuit boards and the like which is equal to or greater than the number of the test pins are provided, resulting in a very large system as a whole. In the conventional semiconductor test system, the printed circuit boards and the like are identical to one another.

For example, in a high speed and high resolution test system, such as a test rate of 500MHz and timing accuracy of 80 picosecond, the printed circuit boards for all the test pins have the same high capabilities each being able to satisfy the test rate and timing accuracy. Thus, the conventional semiconductor test system inevitably becomes a very high cost system. Further, since the identical circuit structure is used in each test pin, the test system can conduct only limited types of test.

An example of devices to be tested includes a type of semiconductor device which has both an analog function and a digital function. A typical example of which is an audio IC or a communication device IC which includes an analog-digital (AD) converter, a digital-analog (DA) converter and a digital signal processing circuit. Further, there is a type of semiconductor device which has a functionality for testing an inner circuit by itself, i.e., built-in self-test (BIST).

In the conventional semiconductor test system, it is constituted so that only one type of functional test can be conducted at one time. Therefore, to test the mixed signal integrated circuit noted above, each functional block must be tested separately in a series fashion, such as, first testing the AD converter, then testing the DA converter, and after that, testing the digital signal processing circuit. Further, in testing the device having the BIST function, such a test for evaluating the BIST function must be carried out separately from the other types of test.

Even in the case where testing a device which is configured solely by logic circuits, almost always, not all of the pins of such a device under test do not require the highest performance of the semiconductor test system. For example, in a typical logic LSI device to be tested having several hundred pins, only several pins actually operate at the highest speed and require the highest speed test signal while other several hundred pins operate at substantially lower speeds and require low speed test signals.

Since the conventional semiconductor test system cannot conduct different types of test in parallel at the same time, it has a drawback that, to complete the mixed signal device test or test of the device having the BIST function, it requires a long test time. Further, the high performance which is needed only for a small number of pins of the device under test is equipped in all of the test pins, resulting in the high cost of the test system.

One of the reasons that the conventional semiconductor test system installs the identical circuit configuration in all of the test pins as noted above, and as a result, not able to conduct two or more different kinds of test at the same time by having different circuit configuration, is that the test system is configured to generate the test pattern by using the cycle based test data. In producing the test pattern using the cycle based concept, the software and hardware tend to be complicated, thus, it is practically impossible to include different circuit configurations and associated software in the test system which would make the test system even more complicated.

To explain the above noted reasons more clearly, brief comparison is made between the test pattern formation using the test data in the cycle based format and the test pattern formation using the test data in the event based format with reference to waveforms shown in FIG. **3**. The more detailed comparison is disclosed in the above noted U.S. patent applications owned by the same assignee of this invention.

The example of FIG. **3** shows the case where a test pattern is created based on the data resulted from the logic simulation conducted in the design stage of the large scale integrated circuit (LSI) and stored in a dump file **37**. The output of the dump file **37** is configured with data in the event based format showing the changes in the input and output of the designed LSI device and having descriptions **38** shown in the lower right of FIG. **3** for expressing, for example, the waveforms **31**.

In this example, it is assumed that test patterns such as shown by the waveforms **31** are to be formed by using such descriptions. The waveforms **31** illustrate test patterns to be generated at pins (tester pins or test channels) Sa and Sb, respectively. The event data describing the waveforms is formed of set edges San, Sbn and their timings (for example, time lengths from a reference point), and reset edges Ran, Rbn and their timings.

For producing a test pattern to be used in the conventional semiconductor test system based on the cycle based concept, the test data must be divided into test cycles (tester rate), waveforms (types of waveforms, and their edge timings), and vectors. An example of such descriptions is shown in the center and left of FIG. **3**. In the cycle based test pattern, as shown by waveforms **33** in the left part of FIG. **3**, a test pattern is divided into each test cycle (TS1, TS2 and TS3) to define the waveforms and timings (delay times) for each test cycle.

An example of data descriptions for such waveforms, timings and test cycles is shown in timing data (test plan) **36**. An example of logic "1", "0" or "Z" of the waveforms is shown in vector data (pattern data) **35**. For example, in the timing data **36**, the test cycle is described by "rate" to define time intervals between test cycles, and the waveform is described by RZ (return to zero), NRZ (non-return to zero) and XOR (exclusive OR). Further, the timing of each waveform is defined by a delay time from a predetermined edge of the corresponding test cycle.

As in the foregoing, because the conventional semiconductor test system produces a test pattern under the cycle based procedure, the hardware structures in the pattern generator, timing generator, and wave formatter tend to be complicated, and accordingly, the software to be used in such hardware becomes complicated as well. Further, since all of the test pins (such as Sa and Sb in the above example) are defined by the common test cycle, it is not possible to generate test patterns of different cycles among the test pins at the same time.

Therefore, in the conventional semiconductor test system, the same circuit configurations are used in all of the test pins, and it is not possible to incorporate printed circuit boards of different circuit structures therein. As a consequence, it is not possible to perform different test such as the analog block test and the digital block test at the same time in a parallel fashion. Moreover, for example, a high speed type test system also needs to include a low speed hardware configuration (such as high voltage and large amplitude generation circuit and a driver inhibit circuit, etc.), the high speed performance cannot be fully improved in such a test system.

In contrast, for producing a test pattern by using the event based method, it is only necessary to read set/reset data and associated timing data stored in an event memory, requiring very simple hardware and software structures. Further, each test pin can operate independently as to whether there is any event therein rather than the test cycle and various types of associated data, thus, test patterns of different functions and frequency ranges can be generated at the same time.

As noted in the foregoing, the inventors of this invention have proposed the event based semiconductor test system. In the event based test system, since the hardware and software involved are very simple in the structure and contents, it is possible to formulate an overall test system having different hardware and software therein. Moreover, since each test pin can operate independently from the other, two or more tests which are different in functions and frequency ranges from one another can be carried out in a parallel fashion at the same time. Further, an application specific and low cost event based test system can be easily established.

SUMMARY OF THE INVENTION

Therefore, it is an object of the present invention to provide a semiconductor test system which is dedicated to a specific application by having tester modules of different capabilities corresponding to test pins and a measurement module to be used for the specific application in a test fixture.

It is another object of the present invention to provide a low cost semiconductor test system which is capable of

testing a semiconductor device having an analog function and a digital function by testing the analog and digital functions in parallel at the same time by incorporating tester modules of different capabilities corresponding to test pins and an analog measurement module in a test fixture.

It is a further object of the present invention to provide a low cost semiconductor test system which is capable of testing a semiconductor device having a BIST (built-in self-test) function and other logic function by testing the BIST and logic functions in parallel at the same time by incorporating tester modules of different capabilities corresponding to test pins and a BIST measurement module in a test fixture.

It is a further object of the present invention to provide a semiconductor test system having tester modules of different capabilities corresponding to test pins wherein interface specification between the test system main frame and the tester modules is standardized for freely accommodating tester modules of different pin counts and performances in the main frame.

It is a further object of the present invention to provide a semiconductor test system which can freely accommodate a plurality of tester modules of different capabilities, thereby being able to carry out tests on a plurality of different kinds of devices or functional blocks at the same time.

It is a further object of the present invention to provide a semiconductor test system which can test a semiconductor device under test at low cost and further enhance its ability depending on the future needs.

The semiconductor test system of the present invention includes two or more tester modules whose performances are different from one another, a test system main frame for installing two or more tester modules therein, a test fixture provided on the test system main frame for electrically connecting the tester modules and a device under test, a measurement module provided in the test fixture for converting signals between the tester modules and the device under test depending on an intended function of the device under test, and a host computer for controlling an overall operation of the test system by communicating with the tester modules through a tester bus.

In the semiconductor test system of the present invention, a measurement module unique to the test application is provided in the test fixture which established electrical connection between the tester modules and the device under test. The test fixture will be replaced depending on the test object. Each of the tester modules includes a plurality of event tester boards. Under the control of the host computer, each tester board provides a test pattern to a corresponding pin of the device under test and evaluates a resultant output signal from the device under test.

In the event based test system of the present invention, the measurement module for a specific test purpose is installed in the test fixture (pin fixture), thereby enabling to simplify the structure of the test modules installed in the test system. Therefore, by replacing test fixtures prepared for specific applications depending on the type of device to be tested or type of test items, an application specific semiconductor test system can be achieved with simple structure and low cost.

In the semiconductor test system of the present invention, since an operation of a test pin is independent from the other test pin, different devices or different blocks in the device can be tested by a group of test pins and other groups of test pins. Thus, by using the application specific test fixtures, an analog circuit and a digital circuit in the device under test can be tested in parallel at the same time. Similarly, the device under test having a BIST function can be easily tested with use of a test fixture having a module which functions as a BIST interface.

As noted above, in the semiconductor test system of the present invention, the tester module (tester board) is configured by event based architecture where all the information required for executing the test is prepared in the event based format. Because it is not necessary to include the rate signal or pattern generator, each test pin in the event based test system can operate independently from the other test pins. Therefore, different types of test, such as analog circuit test and digital circuit test can be performed at the same time.

Further, since the test system of the present invention is configured with a modular basis, a simple and low cost test system can be established depending on the type of test deice or test purpose. Furthermore, because of the event based architecture, the hardware of the event based test system can be dramatically reduced while the software for controlling the tester modules can be dramatically simplified. Accordingly, an overall physical size of the event based test system can be reduced, resulting in further cost reduction, floor space reduction and associated cost savings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a block diagram showing a basic configuration of a semiconductor test system (LSI tester) in the conventional technology.

FIG. **2** is a schematic diagram showing an example of outward appearance of a semiconductor test system in the conventional technology.

FIG. **3** is a diagram for comparing an example of descriptions for producing a cycle based test pattern in the conventional semiconductor test system with an example of descriptions for producing an event based test pattern in the semiconductor test system of the present invention.

FIG. **4** is a block diagram showing an example of test system configuration for testing a mixed signal IC (mixed signal integrated circuit) by an application specific test system of the preset invention.

FIG. **5** is a block diagram showing an example of circuit configuration in an event tester provided in an event tester board which is incorporated in a tester module in accordance with the present invention.

FIG. **6** is a schematic diagram for establishing a semiconductor test system having test pins grouped into different performances by incorporating a plurality of tester modules of the present invention.

FIG. **7A** is a block diagram showing an example of semiconductor test system configured for testing a mixed signal device, and FIG. **7B** is a block diagram showing an example of semiconductor test system configured for testing a BIST function device.

FIG. **8** is a schematic diagram showing an internal structure of a mixed signal IC which is mixed with an analog function and a digital function, and a concept of testing such different functions in the mixed signal device under test in a parallel fashion by the semiconductor test system of the present invention.

FIG. **9A** is a schematic diagram showing a test process for testing the mixed signal device by the conventional semiconductor test system and FIG. **9B** is a schematic diagram showing a test process for testing the mixed signal device by the semiconductor test system of the present invention.

FIG. **10** is a schematic diagram showing an example of outward appearance of the semiconductor test system of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

The embodiment of the present invention is explained with reference to FIGS. **4–10**. FIG. **4** is a block diagram showing a basic structure of the semiconductor test system of the present invention for testing an analog/digital mixed signal integrated circuit ("mixed signal IC" or "mixed signal device). The basic structure of the semiconductor test system for testing the BIST function device is substantially the same as that shown in FIG. **4** except for using a measurement module designed for BIST testing.

In the semiconductor test system of the present invention, a test head (tester main frame) is so configured that one or more modular testers (hereinafter "tester modules") are selectively installed therein. The tester modules to be installed can be a plurality of same tester modules depending on the number of tester pins desired or a combination of different tester modules such as a high speed module HSM and a low speed module LSM.

As will be explained with reference to FIGS. **6** and **7** later, each tester module is provided with a plurality of event tester boards **43**, for example, eight (8) tester boards. Further, each event tester board includes a plurality of event testers **66** corresponding to a plurality of tester pins, such as 32 event testers for 32 tester pins. Therefore, in the example of FIG. **4**, an event tester board $\mathbf{43}_1$ deals with an analog part of the device test while other event tester boards **43** cover a digital part of the device test.

In the test system of FIG. **4**, the plurality of event tester boards **43** are controlled by a tester controller **41**, which is a host computer of the test system, through a system bus **64**. As noted above, for example, eight event tester boards **43** may be installed in one tester module. Although not shown in FIG. **4**, typically, a test system of the present invention is configured by two or more such tester modules as shown in FIG. **6**.

In the test system of FIG. **4**, the event tester board **43** applies a test pattern (test signal) to a device under test **19**, and examines a response signal from the device under test resulted from the test pattern. For testing the analog function of the device under test, an analog measurement (test) module **48** may be provided in the test system. Such an analog measurement module **48** includes, for example, a DA converter, an AD converter and a filter. As will be described later, the analog measurement module **48** is installed in a test fixture (pin fixture) of the test system.

Each event tester board **43** includes event testers $\mathbf{66}_1$–$\mathbf{66}_{32}$ for 32 channels for example, an interface **53**, a processor **67** and a memory **68**. Each event tester **66** corresponds to a tester pin, and has the same inner structure as that of the other within the same tester board. In this example, the event tester **66** includes an event memory **60**, an event execution unit **47**, a driver/comparator **61** and a test result memory **57**.

The event memory **60** stores event data for producing a test pattern. The event execution unit **47** produces the test pattern based on the event data from the event memory **60**. The test pattern is supplied to the device under test **19** through the driver/comparator **61**. In the case where an input pin of the device under test **19** is an analog input, the analog measurement module **48** noted above converts the test pattern to an analog signal by the DA converter therein. Thus, the analog test signal is applied to the device under test **19**. An output signal of the device under test **19** is compared with an expected signal by the driver/comparator **61**, the result of which is stored in the test result memory **57**. In the case where an output signal from the device under test **19** is an analog signal, if necessary, such an analog signal is converted to a digital signal by the AD converter in the analog measurement module **48**.

FIG. **5** is a block diagram showing an example of configuration in the event tester **66** in the event tester board **43** in more detail. The further detailed description regarding the event based test system is given in the above U.S. patent application Ser. No. 09/406,300 as well as U.S. patent application Ser. No. 09/259,401 owned by the same assignee of this invention. In FIG. **5**, the blocks identical to that of FIG. **4** are denoted by the same reference labels.

The interface **53** and the processor **67** are connected to the tester processor (host computer) **41** through the system bus **64**. The interface **53** is used, for example, for transferring data from the tester controller **41** to a register (not shown) in the event tester board to assign the event tester to the input/output pins of the device under test. For example, when the host computer **41** sends a group assigning address to the system bus **64**, the interface **53** interprets the group assigning address and allows the data from the host computer to be stored in the register in the specified event tester board.

The processor **67** is provided, for example, in each event tester board, and controls the operations in the event tester board including generation of events (test patterns), evaluation of output signals from the device under test, and acquisition of failure data. The processor **67** can be provided at each tester board or every several tester boards. Further, the processor **67** may not always necessary be provided in the event tester board, but the same control functions can be made directly by the tester controller **41** to the event tester boards.

An address controller **58** is, for example, in the most simple case, a program counter. The address controller **58** controls the address supplied to the failure data memory **57** and the event memory **60**. The event timing data is transferred to the event memory **60** from the host computer as a test program and stored therein.

The event memory **60** stores the event timing data as noted above which defines timing of each of the events (change points from "1" to "0" and from "0" to "1"). For example, the event timing data is stored as two types of data, one of which shows integer multiples of a reference clock cycle while the other shows fractions of the reference clock cycle. Preferably, the event timing data is compressed before being stored in the event memory **60**.

In the example of FIG. **5**, the event execution unit **47** in FIG. **4** is configured with a decompression unit **62**, a timing count/scaling logic **63**, and an event generator **64**. The decompression unit **62** decompresses (reproduces) the compressed timing data from the event memory **60**. The timing count/scaling logic **63** produces time length data of each event by summing or modifying the event timing data. The time length data expresses the timing of each event by a time length (delay time) from a predetermined reference point.

The event generator **64** produces a test pattern based on the time length data and provides the test pattern to the device under test **19** through the driver/comparator **61**. Thus, a particular pin of the device under test **19** is tested by evaluating the response output therefrom. The driver/comparator **61** is mainly formed with, as shown in FIG. **4**, a driver which drives the test pattern to be applied to the particular device pin and a comparator which determines a voltage level of an output signal of a device pin resultant from the test pattern and compares the output signal with the expected logic data.

In the event tester summarized above, the input signal applied to the device under test and the expected signal compared with the output signal of the device under test are produced by the data in the event based format. In the event based format, the information of change points on the input signal and expected signal is formed of action information (set and/or reset) and time information (time length from a specified point).

As noted above, in the conventional semiconductor test system, the cycle based method has been used, which requires memory capacity smaller than that required in the event based architecture. In the cycle based test system, the time information of the input signal and expected signal is formed of cycle information (rate signal) and delay time information. The action information of the input signal and expected signal is formed of waveform mode data and pattern data. In this arrangement, the delay time information can be defined only by the limited number of data. Further, to generate the pattern data with flexibility, the test program must includes many loops and/or subroutines therein. Therefore, the conventional test system requires complicated structures and operational procedures.

In the event based test system, such complicated structures and operational procedures of the conventional cycle based test system are unnecessary, thereby easily increasing the number of test pins and/or incorporating the test pins of different performances in the same test system. Although the event based test system requires a memory of large capacity, such an increase in the memory capacity is not a major problem since the increase in the memory density and the decrease in the memory cost are rapidly and continuously achieved today.

As in the foregoing, in the event based test system, each of the test pins or each group of test pins can independently perform a test operation from the other. Consequently, in the case where a plurality of different kinds of test have to be performed, such as in testing the mixed signal device under test which includes both analog and digital signals, such different kinds of test can be conducted in a parallel fashion at the same time. Further, start and end timings of such different kinds of test can be independently established.

FIG. **6** is a schematic diagram for establishing a semiconductor test system having test pins grouped into different performances by incorporating a plurality of tester modules of the present invention.

A test head **124** is provided with a plurality of tester modules depending on, for example, the number of pins of a test fixture **127** connected to the test head, a type of device to be tested, and the number of pins of the device to be tested. As will be described later, an interface (connection) specification between the test fixture **127** and the test module is standardized so that any tester modules can be installed in any positions in the test head (system main frame).

The test fixture **127** includes a large number of elastic connectors such as pogo-pins to electrically and mechanically connect the tester modules and a performance board **128**. The device under test **19** is inserted in a test socket on the performance board **128**, thereby establishing an electrical communication with the semiconductor test system. Although not shown in FIG. **6** but is shown in FIGS. **7**A and **7**B, in the present invention, measurement modules specific to the test (such as analog measurement module **48**) are installed in the test fixture **127**. Therefore, the test fixture **127** in the present invention is designed unique to the specific test application.

A performance board **128** is provided on the test fixture **127**. A device under test **19** is inserted, for example, in a test socket on the performance board **128**, thereby establishing electrical communication with the semiconductor test system. As mentioned above, the analog measurement module **48** such as shown in FIG. **4** is installed in the test fixture, however, it also can be mounted on the performance board **128** in a manner similar to the device under test **19**.

Each of the tester module **125** has a predetermined number of pin groups. For example, one high speed module HSM installs printed circuit boards corresponding to 128 test pins (test channels) while one low speed module LSM installs printed circuit boards corresponding to 256 test pins. These numbers are disclosed only for an illustration purpose, and various other numbers of test pins are also possible.

As noted above, each printed circuit board in the tester module has event testers which generates test patterns and applies the same to the corresponding pin of the device under test **19** through the performance board **128**. Output signals of the device under test **19** responsive to the test pattern are transmitted to the event tester board in the tester module through the performance board **128** whereby being compared with the expected signals to determine the pass/fail of the device under test.

Each tester module is provided with an interface (connector) **126**. The connector **126** is so arranged to fit to the standard specification of the test fixture **127**. For example, in the standard specification of the test fixture **127**, a structure of connector pins, impedance of the pins, distance between the pins (pin pitch), and relative positions of the pins are specified for the intended test head. By using the interface (connector) **126** which matches the standard specification on all of the tester modules, test systems of various combinations of the tester modules can be freely established.

Because of the configuration of the present invention, a test system of optimum cost/performance which matches the device under test can be established. Further, improvement of the performance of the test system can be achieved by replacing one or more test modules, thus, an overall life time of the test system can be increased. Moreover, the test system of the present invention can accommodate a plurality of test modules whose performances are different from the other, and thus, the desired performance of the test system can be achieve directly by the corresponding test modules. Therefore, the performance of the test system can be easily and directly improved.

FIG. **7**A is a block diagram showing an example of semiconductor test system configured for testing a mixed signal device, and FIG. **7**B is a block diagram showing an example of semiconductor test system configured for testing a BIST function device. For simplicity of illustration, the interface **126** in FIG. **6** is not shown here. Further, the tester modules **125** are simply denoted by TM, although each of which may be same or different from one another depending on the purpose of the test.

The semiconductor test system of FIG. **7**A is so configured that it is dedicated to a device under test which has an analog circuit therein. Accordingly, analog measurement (test) modules **132** and **133** are provided in the test fixture **127**. For example, when a particular input pin of the device under test is an analog signal pin, a test signal from the tester module **125** is converted to an analog signal by the analog measurement (test) module **133** having a DA converter. Thus, the analog test signal is applied to the particular input pin of the device under test. Further, when a particular output pin of the device under test is an analog signal pin, the output signal from the output pin is converted to a digital signal by

the analog measurement (test) module **132** having an AD converter. Thus, the digital output signal is transmitted to the tester module **125**.

As in the foregoing, the application of the test fixture in the test system of the present invention is limited to a specific test object. Accordingly, the tester modules **125** can be completely separated from the analog functions and be designed to deal with only digital signals. Thus, overall cost of the test system can be substantially decreased. Moreover, an interface structure between the tester modules and the test fixtures is simplified.

Other example of the analog measurement module includes an audio signal source, audio digitizer, video signal source, video digitizer, and associated circuits such as filters. Further, a card interface, such as for an IC card (smart card) can be installed in the test fixture **127**. In such an arrangement, an IC card under test can be connected to the card interface and be tested without involving the performance board **128**.

The semiconductor test system of FIG. **7B** is so configured that it is dedicated to a device under test having a BIST (built-in self-test) function therein. An IC device having such a BIST function includes a BIST controller which interfaces between test system and the inner circuit of the device during the test. As defined by IEEE Std. 1149.1 "Standard Test Access Port and Boundary-Scan Architecture", the BIST controller and the test system communicate with each other through the interface formed of five pins, i.e., an interface pin group.

This interface pin group needs to have high speed operation capability. In the example of FIG. **7B**, a BIST module **134** having the interface pin group is provided in the test fixture **127**. By this arrangement, an application specific test system which can test an IC device having the BIST function can be established with low cost.

FIG. **8** is a block diagram showing a basic concept for conducting different types of test in parallel for a mixed signal device **19** having analog and digital functions by the semiconductor test system of the present invention. In this example, the mixed signal device **19** includes an AD converter circuit, a logic circuit, and a DA converter circuit. The semiconductor test system of the present invention can perform test for each group of specified number of tester pins independently from the other group as noted above. Therefore, by assigning the groups of tester pins to these circuits in the mixed signal device, these circuits can be tested in parallel at the same time.

FIG. **9A** is a schematic diagram showing a test process for testing the mixed signal device by the conventional semiconductor test system and FIG. **9B** is a schematic diagram showing a test process for testing the mixed signal device by the semiconductor test system of the present invention. When testing the mixed signal IC having analog and digital circuits such as shown in FIG. **8** by the conventional semiconductor test system, the test must proceed in a series fashion such as completing one test and moving to the next test. Therefore, the overall time required for completing the test is the sum of times of all of the tests as shown in FIG. **9A**.

In contrast, when testing the mixed signal IC shown in FIG. **8** by the semiconductor test system of the present invention, the AD converter circuit, logic circuit and DA converter circuit can be tested in parallel at the same time as shown in FIG. **9B**. Thus, the present invention can dramatically reduce the overall test time. Since it is a common practice to evaluate the test result of the AD converter circuit or DA converter circuit by predetermined formulas, a computation time after each of the AD and DA circuit test is provided in FIGS. **9A** and **9B**.

An example of outer appearance of the semiconductor test system of the present invention is shown in the schematic diagram of FIG. **10**. In the example of FIG. **10**, a host computer (main system computer) **41** is, for example, a work station having a graphic user interface (GUI). The host computer **41** functions as a user interface as well as a controller to control an overall operation of the test system. The host computer **41** and the inner hardware of the test system are connected through the system bus **64** (FIGS. **4** and **5**).

The event based test system of the present invention does not need the pattern generator and the timing generator used in the conventional semiconductor test system configured by the cycle based concept. Therefore, it is possible to substantially decrease the physical size of the overall test system by installing all of the modular event testers in the test head (or tester main frame) **124**.

As has been foregoing, in the event based test system of the present invention, the test fixture (pin fixture) installs the measurement (test) modules designed for specific applications, thereby simplifying the tester modules to be inserted in the test system. Accordingly, by replacing the test fixtures prepared based on the specific applications, it is easily able to establish a semiconductor test system of simple and low cost.

In the event based semiconductor test system of the present invention noted above, each test pin can operate independently from the other test pins. Thus, by assigning groups of test pins to different devices or blocks under test, two or more different devices or blocks can be tested at the same time. Therefore, according to the event based test system of the present invention, an analog circuit and a digital circuit in a mixed signal device can be tested in parallel at the same time. Further, the test system of the present invention can evaluate the IC device having the BIST function by using the test fixture having the BIST module which works as the BIST interface.

As noted above, in the semiconductor test system of the present invention, the tester module (tester board) is configured by event based architecture where all the information required for executing the test is prepared in the event based format. Therefore, different types of test, such as analog circuit test and digital circuit test can be performed at the same time.

Since the semiconductor test system of the present invention has a modular structure, a desired test system can be formed freely depending on the kind of devices to be tested and the purpose of the test. Further, the hardware of the event based test system can be dramatically reduced while the software for the test system can be dramatically simplified. Accordingly, the tester modules of different capabilities and performances can be installed together in the same test system. Furthermore, as shown in FIG. **6**, an overall physical size of the event based test system can be considerably reduced, resulting in further cost reduction, floor space reduction and associated cost savings.

What is claimed is:

1. A semiconductor test system, comprising:

two or more tester modules whose performances are identical to or different from one another;

a test system main frame for accommodating an arbitrary combination of the tester modules therein;

a test fixture provided on the test system main frame for electrically connecting the tester modules and a device under test;

a measurement module provided in the test fixture for converting signals between the device under test and the tester module depending on a function of the device under test; and

a host computer for controlling an- overall operation of the test system by communicating with the tester modules in the test system through a tester bus.

2. A semiconductor test system as defined in claim 1, wherein a plurality of test fixtures are prepared which install the measurement modules with different types depending on kinds of devices to be tested, and the test fixture selected on the basis of the kinds of device under test is installed in the test system during the test.

3. A semiconductor test system as defined in claim 1, wherein the measurement module includes a function for converting between an analog signal and a digital signal when the device under test is an analog and digital mixed signal integrated circuit.

4. A semiconductor test system as defined in claim 1, wherein the measurement module includes a function for interfacing with a BIST (built-in self-test) controller in the device under test when the device under test has a BIST function.

5. A semiconductor test system as defined in claim 1, wherein specification for connecting the test fixture and the tester module is standardized.

6. A semiconductor test system as defined in claim 1, wherein the test fixture includes a performance board having a mechanism for mounting the device under test thereon and a connection mechanism for electrically connecting between the performance board and the tester modules.

7. A semiconductor test system as defined in claim 1, wherein a number of tester pins is variably assigned to the tester module.

8. A semiconductor test system as defined in claim 1, wherein a number of tester pins is variably assigned to the tester module, and such assignment of test pins and modification thereof are regulated by address data from the host computer.

9. A semiconductor test system as defined in claim 1, wherein each of the tester modules includes a plurality of event tester boards where each of the event tester boards is assigned to a predetermined number of test pins.

10. A semiconductor test system as defined in claim 1, wherein each of the tester modules includes an inner controller where the inner controller controls, in response to instructions from the host computer, to generate a test pattern from the tester module and to evaluate an output signal of the device under test.

11. A semiconductor test system as defined in claim 9, wherein each of the tester modules includes a plurality of event tester boards wherein each of the event tester boards includes an inner controller where the inner controller controls, in response to instructions from the host computer, to generate a test pattern from the tester module and to evaluate an output signal of the device under test.

12. A semiconductor test system as defined in claim 1, wherein each of the tester modules includes a plurality of event tester boards where each of the event tester boards is assigned to one test pin, wherein each of the event tester boards is comprised of:

a controller which controls, in response to instructions from the host computer, to generate the test pattern from the tester module and to evaluate an output signal of the device under test;

an event memory for storing timing data for each event;

an address sequencer for providing, under the control of the controller, address data to the event memory;

means for producing a test pattern based on the timing data from the event memory; and

a driver/comparator for transferring the test pattern to a corresponding pin of the device under test and receiving a response output signal from the device under test.

* * * * *

Address Sequencer (program counter) (Claim)
DACs, ADCs
>1 DUTs @ same time

US006536006B1

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Sugamori

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(54) **EVENT TESTER ARCHITECTURE FOR MIXED SIGNAL TESTING**

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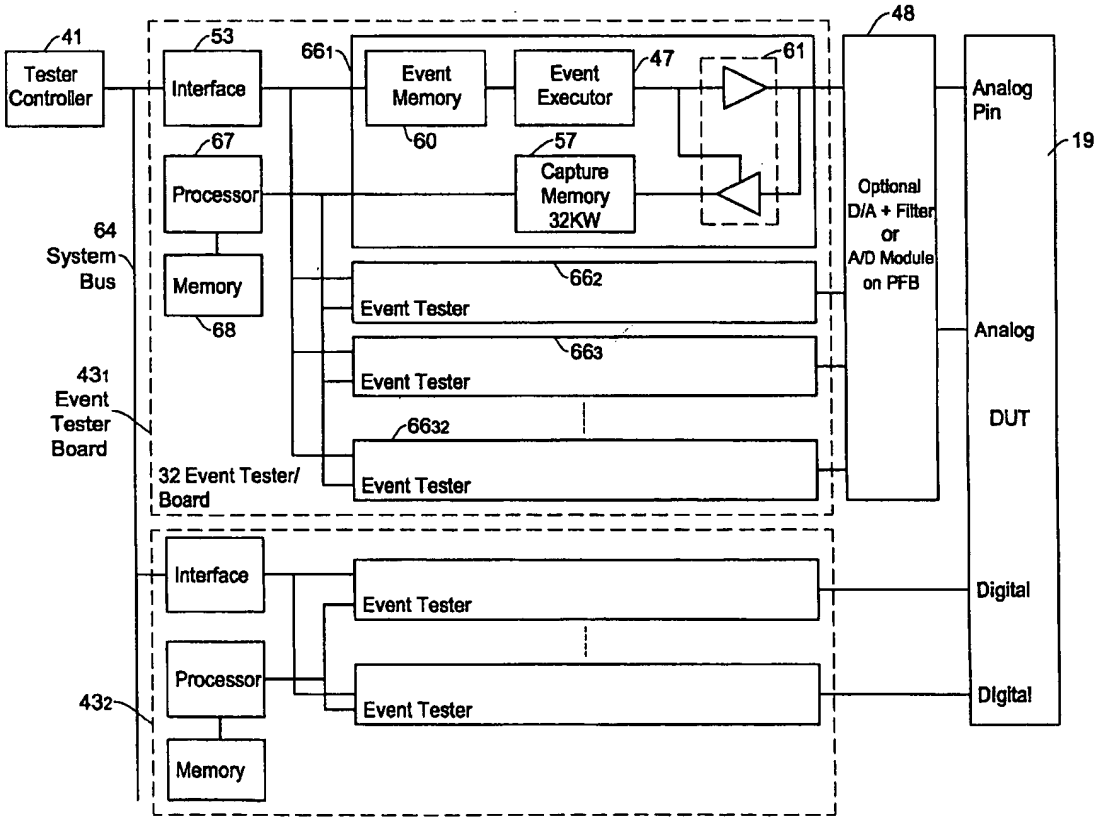
(57) **ABSTRACT**

A semiconductor test system having a plurality of different types of tester modules for testing a mixed signal integrated circuit (IC) having analog signals and digital signals with high speed and high efficiency. The semiconductor test system includes two or more tester modules whose performances are different from one another, a test head to accommodate the two or more tester modules, means provided on the test head for electrically connecting the tester modules and a device under test, an optional circuit corresponding to the device under test when the device under test is a mixed signal IC, and a host computer for controlling an overall operation of the test system. Each event tester module includes a tester board which is configured as an event based tester.

11 Claims, 9 Drawing Sheets



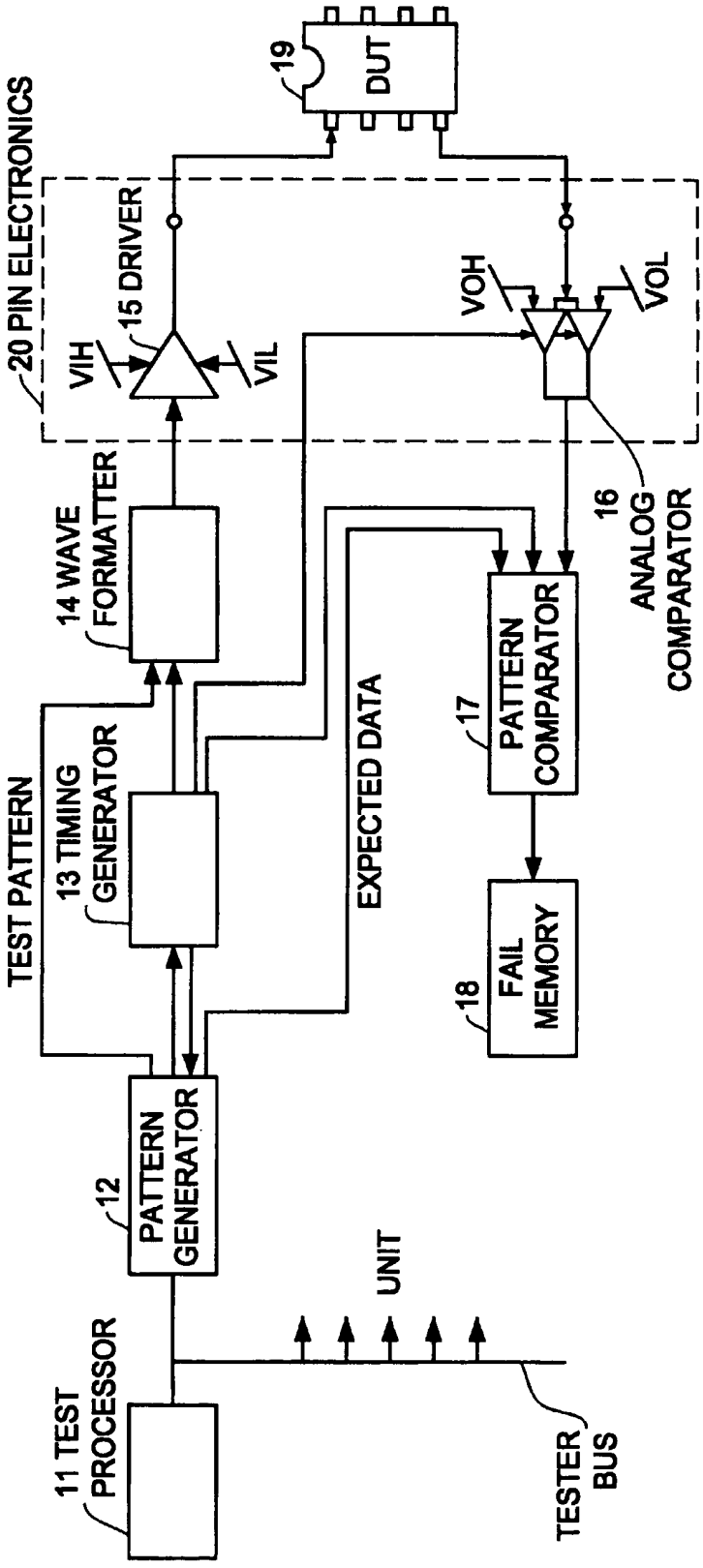
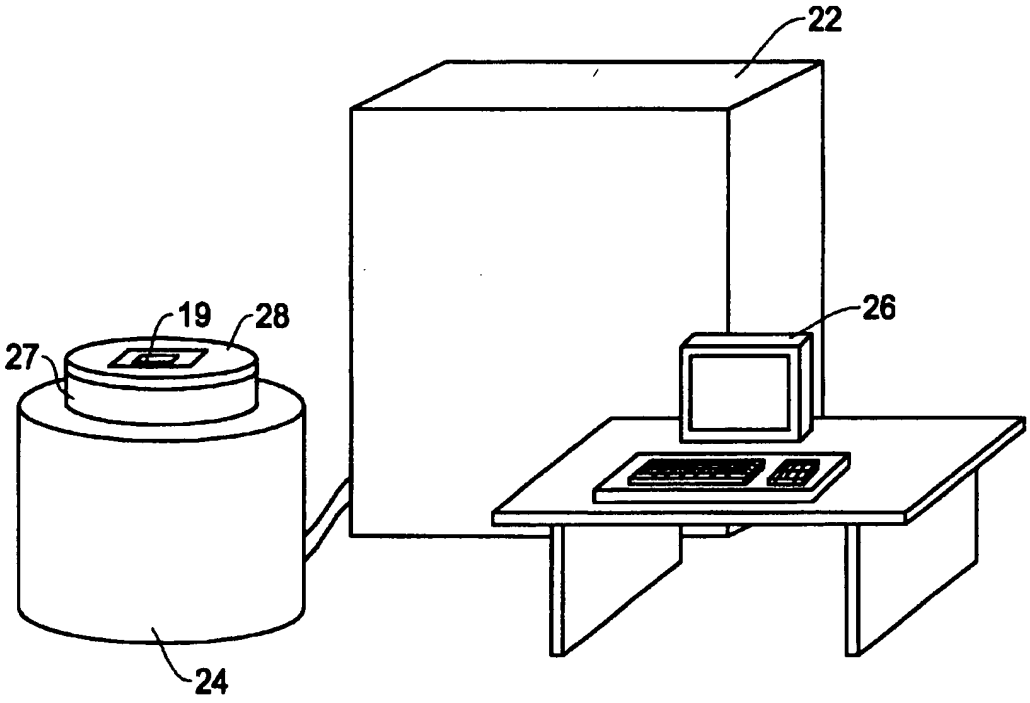


Fig. 1 (Prior Art)

Fig. 2 (Prior Art)



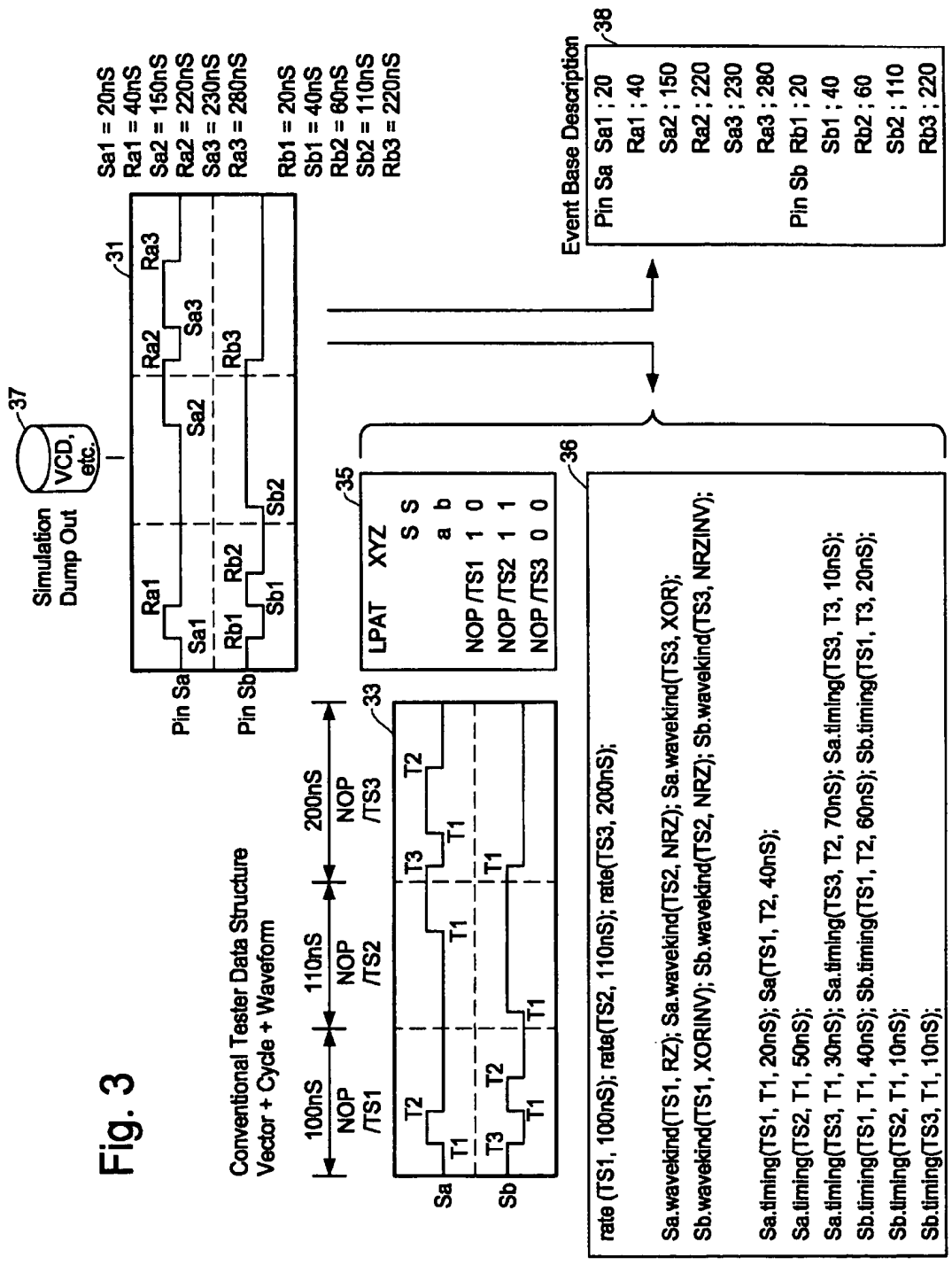

Sa1 = 20nS
Ra1 = 40nS
Sa2 = 150nS
Ra2 = 220nS
Sa3 = 230nS
Ra3 = 280nS
Rb1 = 20nS
Sb1 = 40nS
Rb2 = 80nS
Sb2 = 110nS
Rb3 = 220nS
37
VCD, etc.
Simulation Dump Out
31
Ra1
Ra2
Ra3
Sa1
Sa2
Sa3
Rb1
Rb2
Rb3
Sb1
Sb2
Pin Sa
Pin Sb
Event Base Description
38
Pin Sa Sa1 ; 20
Ra1 ; 40
Sa2 ; 150
Ra2 ; 220
Sa3 ; 230
Ra3 ; 280
Pin Sb Rb1 ; 20
Sb1 ; 40
Rb2 ; 60
Sb2 ; 110
Rb3 ; 220
35
LPAT XYZ
S S
a b
NOP /TS1 1 0
NOP /TS2 1 1
NOP /TS3 0 0
36
rate (TS1, 100nS); rate(TS2, 110nS); rate(TS3, 200nS);
Sa.wavekind(TS1, RZ); Sa.wavekind(TS2, NRZ); Sa.wavekind(TS3, XOR);
Sb.wavekind(TS1, XORINV); Sb.wavekind(TS2, NRZ); Sb.wavekind(TS3, NRZINV);
Sa.timing(TS1, T1, 20nS); Sa(TS1, T2, 40nS);
Sa.timing(TS2, T1, 50nS);
Sa.timing(TS3, T1, 30nS); Sa.timing(TS3, T2, 70nS); Sa.timing(TS3, T3, 10nS);
Sb.timing(TS1, T1, 40nS); Sb.timing(TS1, T2, 60nS); Sb.timing(TS1, T3, 20nS);
Sb.timing(TS2, T1, 10nS);
Sb.timing(TS3, T1, 10nS);
Conventional Tester Data Structure
Vector + Cycle + Waveform
100nS NOP /TS1
110nS NOP /TS2
200nS NOP /TS3
33
Sa
Sb
T1
T2
T3

Fig. 3

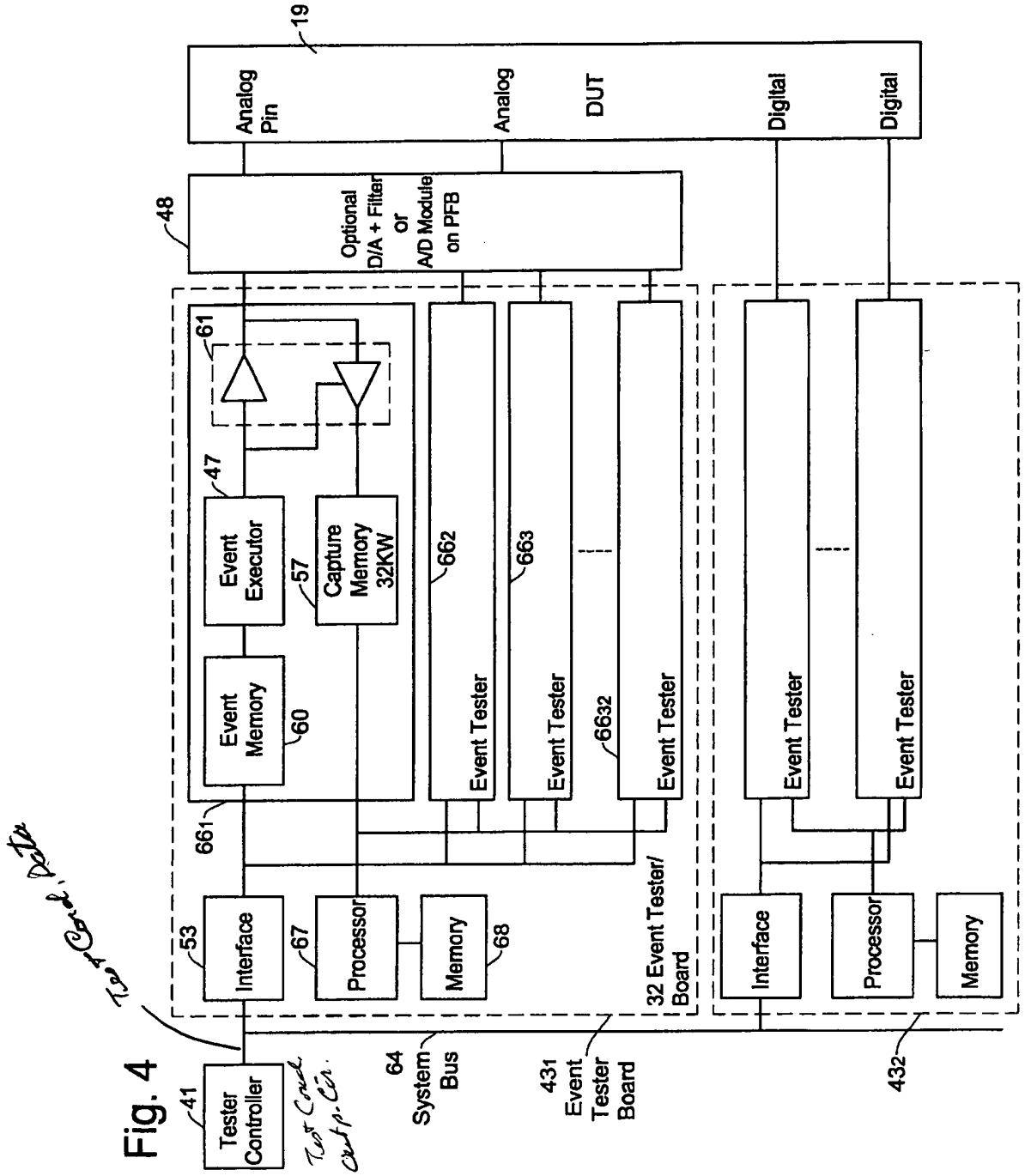

19
Analog Pin
Analog
DUT
Digital
Digital
48
Optional D/A + Filter or A/D Module on PFB
61
47
Event Executor
57
Capture Memory 32KW
Event Memory
60
662
663
6632
Event Tester
661
53
Interface
67
Processor
68
Memory
32 Event Tester/ Board
41
Tester Controller
64
System Bus
431
Event Tester Board
432

Fig. 4

Fig. 5

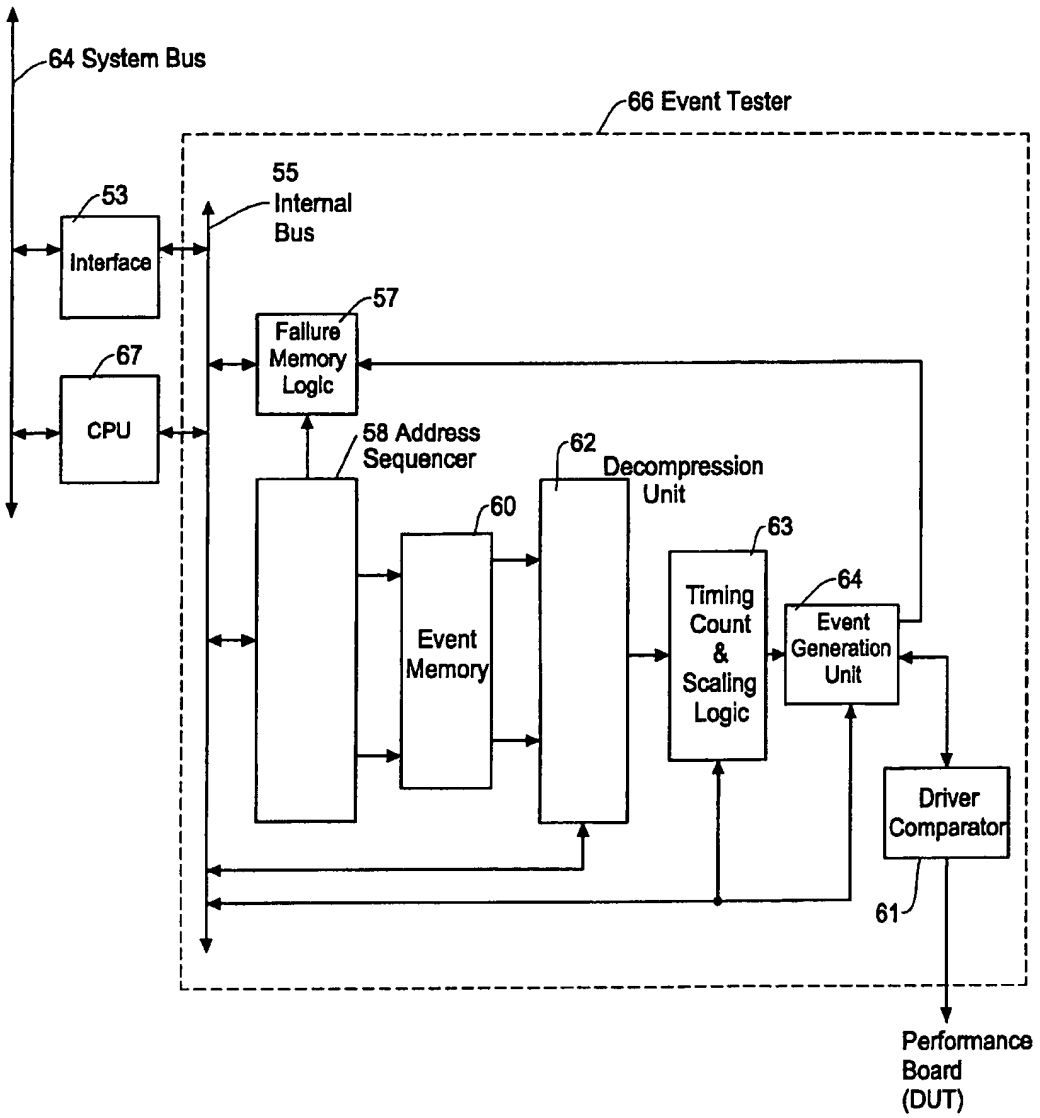

64 System Bus
66 Event Tester
55
Internal
Bus
53
Interface
57
Failure
Memory
Logic
67
CPU
58 Address
Sequencer
62
Decompression
Unit
60
63
Timing
Count
&
Scaling
Logic
64
Event
Generation
Unit
Event
Memory
Driver
Comparator
61
Performance
Board
(DUT)

Fig. 6

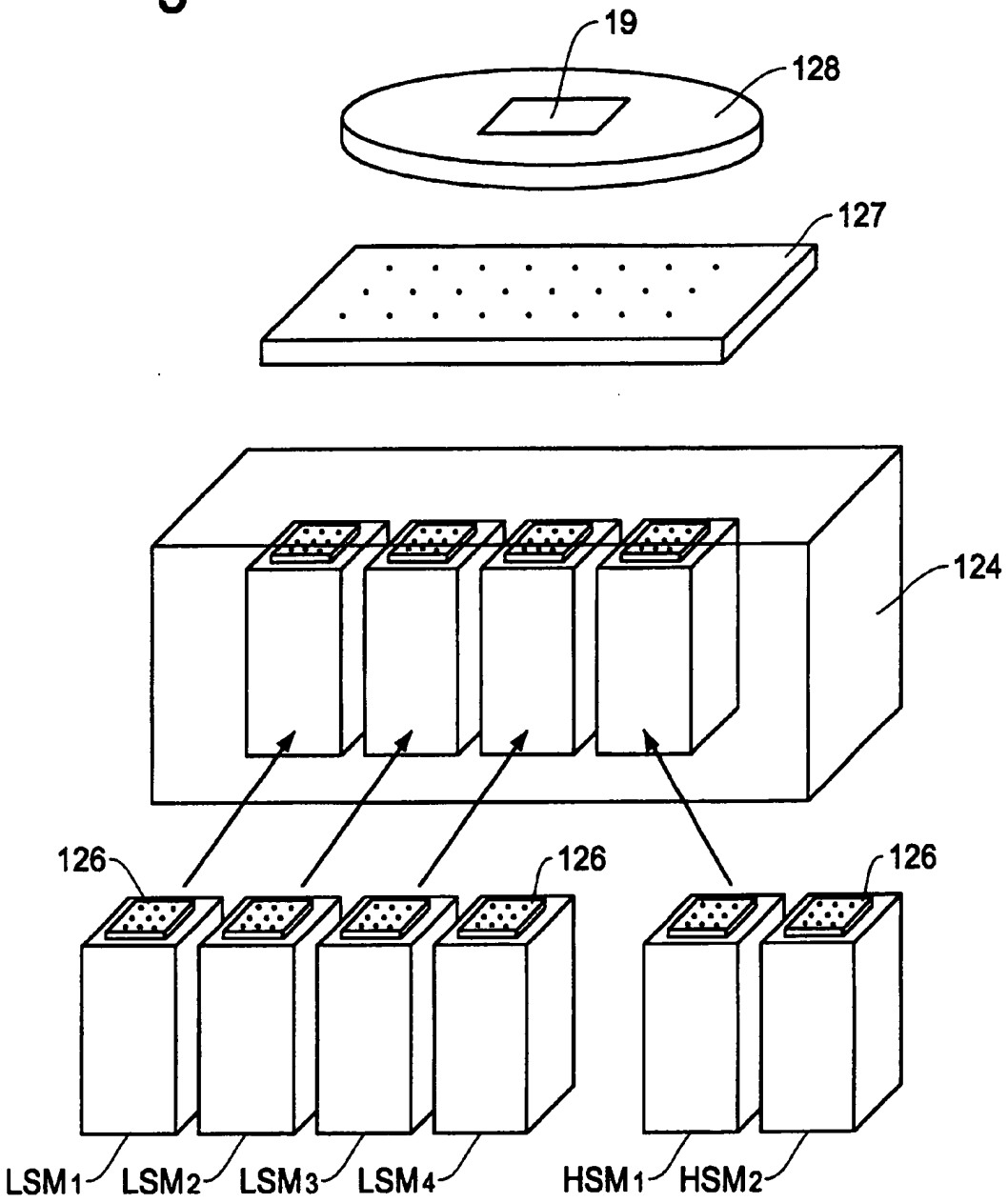


Fig. 7

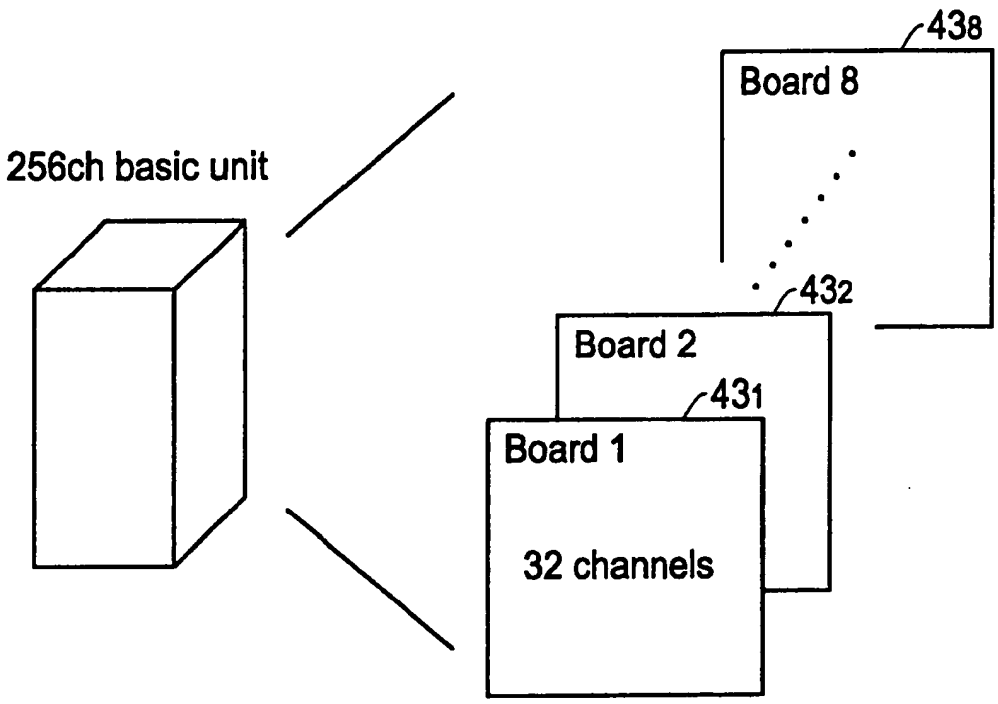

256ch basic unit
438
Board 8
432
Board 2
431
Board 1
32 channels

Fig. 8

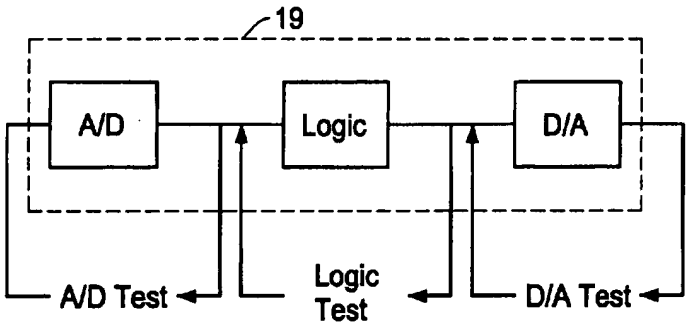


Fig. 9A

Fig. 9B

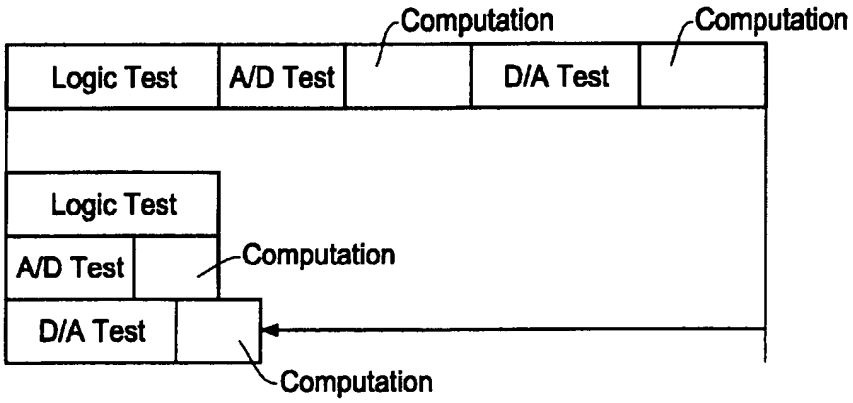
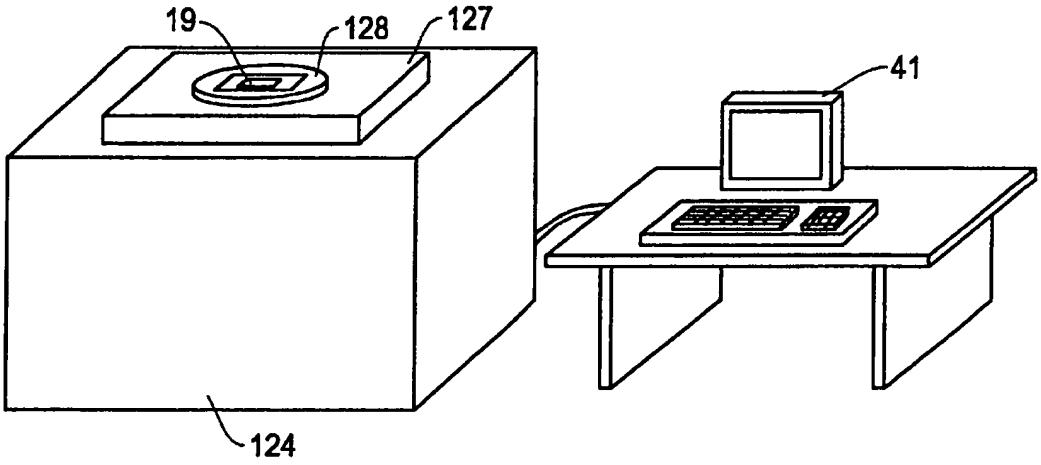


Fig. 10



EVENT TESTER ARCHITECTURE FOR MIXED SIGNAL TESTING

FIELD OF THE INVENTION

This invention relates to a semiconductor test system for testing semiconductor integrated circuits such as a large scale integrated (LSI) circuit, and more particularly, to a semiconductor test system having an event tester architecture which is capable of testing a mixed signal integrated circuit with high speed and high efficiency. In the semiconductor test system of the present invention, a test system is formed by freely combining a plurality of tester modules having identical or different capabilities where each of the tester module operates independently from one another thereby being able to test an analog signal block and a digital signal block of the device under test at the same time.

BACKGROUND OF THE INVENTION

FIG. 1 is a schematic block diagram showing an example of a semiconductor test system in the conventional technology for testing a semiconductor integrated circuit (hereafter may also be referred to as "IC device", "LSI under test" or "device under test").

In the example of FIG. **1**, a test processor **11** is a dedicated processor provided within the semiconductor test system for controlling the operation of the test system through a tester bus. Based on pattern data from the test processor **11**, a pattern generator **12** provides timing data and waveform data to a timing generator **13** and a wave formatter **14**, respectively. A test pattern is produced by the wave formatter **14** with use of the waveform data from the pattern generator **12** and the timing data from the timing generator **13**, and the test pattern is supplied to a device under test (DUT) **19** through a driver **15**.

A response signal from the DUT **19** resulted from the test pattern is converted to a logic signal by an analog comparator **16** with reference to a predetermined threshold voltage level. The logic signal is compared with expected value data from the pattern generator **12** by a logic comparator **17**. The result of the logic comparison is stored in a failure memory **18** corresponding to the address of the DUT **19**. The driver **15**, the analog comparator **16** and switches (not shown) for changing pins of the device under test, are provided in a pin electronics **20**.

The circuit configuration noted above is provided to each test pin of the semiconductor test system. Therefore, since a large scale semiconductor test system has a large number of test pins, such as from 256 test pins to 1024 test pins, and the same number of circuit configurations each being shown in FIG. **1** are incorporated, an actual semiconductor test system becomes a very large system. FIG. **2** shows an example of outer appearance of such a semiconductor test system. The semiconductor test system is basically formed with a main frame **22**, a test head **24**, and a work station **26**.

The work station **26** is a computer provided with, for example, a graphic user interface (GUI) to function as an interface between the test system and a user. Operations of the test system, creation of test programs, and execution of the test programs are conducted through the work station **26**.

The main frame **22** includes a large number of test pins (test channels) each having the test processor **11**, pattern generator **12**, timing generator **13**, wave formatter **14** and comparator **17** shown in FIG. **1**.

The test head **24** includes a large number of printed circuit boards each having the pin electronics **20** shown in FIG. **1**. The test head **24** has, for example, a cylindrical shape in which the printed circuit boards forming the pin electronics are radially aligned. On an upper surface of the test head **24**, a device under test **19** is inserted in a test socket at about the center of a performance board **28**.

Between the pin electronics circuit and the performance board **28**, a pin (test) fixture **27** is provided which is a contact mechanism for communication of electrical signals. The pin fixture **27** includes a large number of contactors such as pogo-pins for electrically connecting the pin electronics circuits and the performance board. The device under test **19** receives a test pattern signal from the pin electronics and produces a response output signal.

In the conventional semiconductor test system, for producing a, test pattern to be applied to a device under test, the test data which is described by, what is called a cycle based format, has been used. In the cycle based format, each variable in the test pattern is defined relative to each test cycle (tester rate) of the semiconductor test system. More specifically, test cycle (tester rate) descriptions, waveform (kinds of waveform, edge timings) descriptions, and vector descriptions in the test data specify the test pattern in a particular test cycle.

In the design stage of the device under test, under a computer aided design (CAD) environment, the resultant design data is evaluated by performing a logic simulation process through a testbench. However, the design evaluation data thus obtained through the testbench is described in an event based format. In the event based format, each change point (event) in the particular test pattern, such as from "0" to "1" or from "1" to "0", is described with reference to a time passage. The time passage is expressed by, for example, an absolute time length from a predetermined reference point or a relative time length between two adjacent events.

The inventor of this invention has disclosed the comparison between the test pattern formation using the test data in the cycle based format and the test pattern formation using the test data in the event based format in the U.S. patent application Ser. No. 09/340,371. The inventor of this invention has also proposed an event based test system as a semiconductor test system as a new concept test system. The details of the structure and operation of the event based test system is given in the U.S. patent application Ser. No. 09/406,300 owned by the same assignee of this invention.

As described in the foregoing, in the semiconductor test system, a large number of printed circuit boards and the like which is equal to or greater than the number of the test pins are provided, resulting in a very large system as a whole. In the conventional semiconductor test system, the printed circuit boards and the like are identical to one another.

For example, in a high speed and high resolution test system, such as a test rate of 500 MHz and timing accuracy of 80 picosecond, the printed circuit boards for all the test pins have the same capabilities each being able to satisfy the

test rate and timing accuracy. Thus, the conventional semiconductor test system inevitably becomes a very high cost system. Further, since the identical circuit structure is used in each test pin, the test system can conduct only limited types of test.

An example of devices to be tested includes a type of semiconductor device which has both an analog function and a digital function. A typical example of which is an audio IC or a communication device IC which includes an analog-digital (AD) converter, a digital-analog (DA) converter and a digital signal processing circuit. In the conventional semiconductor test system, only one type of functional test must be conducted at one time. Therefore, to test the mixed signal integrated circuit noted above, each functional block must be tested separately in a series fashion, such as, first testing the AD converter, then testing the DA converter, and after that, testing the digital signal processing circuit.

Even in the case where testing a device which is configured solely by logic circuits, almost always, not all of the pins of such a device under test require the highest performance of the semiconductor test system. For example, in a typical logic LSI device to be tested having several hundred pins, only several pins actually operate at the highest speed and require the highest speed test signal while other several hundred pins operate at substantially lower speed and require low speed test signals. This is also true to a system-on-chip (SoC), a recent semiconductor device which draws high attention. Thus, high speed test signals must be applied to only a small number of pins of SoC while low speed test signals are sufficient for other pins.

Since the conventional semiconductor test system cannot conduct different types of test in parallel at the same time, it has a drawback that, to complete the mixed signal device test, it requires a long time. Further, the high performance which is needed only for a small number of pins of the device under test is equipped to all of the test pins, resulting in the high cost of the test system.

One of the reasons that the conventional semiconductor test system installs the identical circuit configuration in all of the test pins as noted above, and as a result, are not able to conduct two or more different kinds of test at the same time by having different circuit configuration, is that the test system is configured to generate the test pattern by using the cycle based test data. In producing the test pattern using the cycle based concept, the software and hardware tend to be complicated even when using the same circuit configuration for all the test channels. Thus, it is practically impossible to include different circuit configurations in the test system because it would make the test system and associated software even more complicated.

To explain the above noted reason more clearly, brief comparison is made between the test pattern formation using the test data in the cycle based format and the test pattern formation using the test data in the event based format with reference to waveforms shown in FIG. **3**. The more detailed comparison is disclosed in the above noted U.S. patent applications owned by the same assignee of this invention.

The example of FIG. **3** shows the case where a test pattern is created based on the data resulted from the logic simulation conducted in the design stage of the integrated circuit and stored in a dump file (VCD) **37**. The output of the dump file is data in the event based format showing the changes in the input and output of the designed LSI (large scale integrated circuit) device and having descriptions **38** shown in the lower right of FIG. **3** for expressing, for example, the waveforms **31**.

In this example, it is assumed that test patterns such as shown by the waveform **31** are to be formed by using such descriptions. The waveforms **31** illustrate test patterns to be generated by pins (tester pins or test channels) Sa and Sb, respectively. The event data describing the waveforms is formed of set edges San, Sbn and their timings (for example, time lengths from a reference point), and reset edges Ran, Rbn and their timings.

For producing a test pattern to be used in the conventional semiconductor test system based on the cycle based concept, the test data must be divided into test cycles (tester rate), waveforms (types of waveforms, and their edge timings), and vectors. An example of such descriptions is shown in the center and left of FIG. **3**. In the cycle based test pattern, as shown by waveforms **33** in the left part of FIG. **3**, a test pattern is divided into each test cycle (TS1, TS2 and TS3) to define the waveforms and timings (delay time) for each test cycle.

An example of data descriptions for such waveforms, timings and test cycles is shown in timing data (test plan) **36**. An example of logic "1", "0" or "Z" of the waveforms is shown in vector data (pattern data) **35**. For example, in the timing data **36**, the test cycle is described by "rate" to define time intervals between test cycles, and the waveform is described by RZ (return to zero), NRZ (non-return to zero) and XOR (exclusive OR). Further, the timing of each waveform is defined by a delay time from a predetermined edge of the corresponding test cycle.

As in the foregoing, because the conventional semiconductor test system produces a test pattern under the cycle based procedure, the hardware structures in the pattern generator, timing generator, and wave formatter tend to be complicated, and accordingly, the software to be used in such hardware also becomes complicated as well. Further, since all of the test pins (such as Sa and Sb in the above example) are defined by the common test cycle, it is not possible to generate test patterns of different cycles among the test pins at the same time.

Therefore, in the conventional semiconductor test system, the same circuit configurations are used in all of the test pins, and it is not possible to incorporate printed circuit boards of different circuit structures therein. As a consequence, it is not possible to perform different test such as the analog block test and the digital block test at the same time in a parallel fashion. Moreover, for example, a high speed type test system also needs to include a low speed hardware configuration (such as high voltage and large amplitude generation circuit and a driver inhibit circuit, etc.), the high speed performance cannot be fully improved in such a test system.

In contrast, for producing a test pattern by using the event based method, it is only necessary to read set/reset data and associated timing data stored in an event memory, requiring very simple hardware and software structures. Further, each

test pin can operate independently as to whether there is any event therein rather than the test cycle, thus, test patterns of different functions and frequency ranges can be generated at the same time.

As noted in the foregoing, the inventors of this invention have proposed the event based semiconductor test system. In the event based test system, since the hardware and software involved are very simple in the structure and contents, it is possible to formulate an overall test system having different hardware and software therein. Moreover, since each test pin can operate independently from the other, two or more tests which are different in functions and frequency ranges from one another can be carried out in a parallel fashion at the same time.

SUMMARY OF THE INVENTION

Therefore, it is an object of the present invention to provide a semiconductor test system which has tester modules of different capabilities corresponding to test pins and thus is capable of testing a mixed signal device under test by testing the analog function and the digital function in parallel at the same time.

It is another object of the present invention to provide a semiconductor test system in which tester modules of different pin numbers and capabilities can freely installed in a tester main frame (or test head) and in which specification for connection between the tester modules and the tester main frame is standardized.

It is a further object of the present invention to provide a semiconductor test system which can freely accommodate a plurality of tester modules of different capabilities, thereby testing a plurality of different kinds of devices or functional blocks under test in parallel at the same time.

It is a further object of the present invention to provide a semiconductor test system which can freely accommodate a plurality of tester modules of different capabilities, thereby establishing a test system having a sufficient test performance with low cost, and further enabling to improve its capability in the future.

The semiconductor test system of the present invention includes two or more tester modules whose performances are different from one another, a test head to accommodate the two or more tester modules having different performances, means provided on the test head for electrically connecting the tester modules and a device under test, an optional circuit corresponding to the device under test when the device under test is a mixed signal IC having analog and digital functions, and a host computer for controlling an overall operation of the test system by communicating with the tester modules through a tester bus. One type of the performances of the tester module is a high speed and high timing resolution while other type of performance is a low speed and low timing resolution.

In the semiconductor test system of the present invention, each of the tester modules includes a plurality of event tester boards. Under the control of the host computer, each tester board provides a test pattern to a corresponding pin of the device under test and evaluates a resultant output signal from the device under test.

Since the semiconductor test system of the present invention has a modular structure, a desired test system can be formed freely depending on the kind of devices to be tested and the purpose of the test. Thus, when the device under test is a mixed signal integrated circuit (having both an analog circuit and a digital circuit therein), the analog circuit and the digital circuit can be tested in parallel at the same time. When the device under test is a high speed logic IC, only a small portion of the logic circuits therein are actually operating in the high speed. Thus, for testing such a high speed logic IC, a small number of tester pins have to have high speed capability. In the semiconductor test system of the present invention, the specification for connecting the test head and tester modules (interface) is standardized. Accordingly, any tester modules having the standard interface can be installed at any positions in the test head.

As noted above, in the semiconductor test system of the present invention, the tester module (tester board) is configured by event based architecture where all the information required for executing the test is prepared in the event based format. Therefore, the rate signal showing the start timing of each test cycle or the pattern generator which operates in synchronism with the rate signal used in the conventional technology are no longer necessary. Because it is not necessary to include the rate signal or pattern generator, each test pin in the event based test system can operate independently from the other test pins. Therefore, different types of test, such as analog circuit test and digital circuit test can be performed at the same time.

Further, because of the event based architecture, the hardware of the event based test system can be dramatically reduced while the software for controlling the tester modules can be dramatically simplified. Accordingly, an overall physical size of the event based test system can be reduced, resulting in further cost reduction, floor space reduction and associated cost savings.

Further in the semiconductor test system of the present invention, the logic simulation data in the design stage of the device in the electronic design automation (EDA) environment can be directly used to produce the test pattern to test the device in the evaluation stage. Thus, a turnaround time between the design of the device and the evaluation of the device can be substantially decreased, thereby further decreasing the test cost while increasing the test efficiency.

BRIEF DESCRIPTION IF THE DRAWINGS

FIG. **1** is a block diagram showing a basic configuration of a semiconductor test system (LSI tester) in the conventional technology.

FIG. **2** is a schematic diagram showing an example of outward appearance of a semiconductor test system in the conventional technology.

FIG. **3** is a diagram for comparing an example of descriptions for producing a cycle based test pattern in the conventional semiconductor test system with an example of descriptions for producing an event based test pattern in the semiconductor test system of the present invention.

FIG. **4** is a block diagram showing an example of test system configuration for testing admixed signal IC (mixed signal integrated circuit) by a semiconductor test system of the present invention.

FIG. **5** is a block diagram showing an example of circuit configuration in an event tester provided in an event tester

board which is incorporated in a tester module in accordance with the present invention.

FIG. **6** is a schematic diagram for establishing a semiconductor test system having test pins grouped into different performances by incorporating a plurality of tester modules of the present invention.

FIG. **7** is a block diagram showing an example of tester module which is comprised of a plurality of event tester boards to be used in the semiconductor test system of the present invention.

FIG. **8** is a schematic diagram showing an internal structure of a mixed signal IC which is mixed with an analog function and a digital function, and a concept of testing such different functions in the mixed signal device under test in a parallel fashion by the semiconductor test system of the present invention.

FIG. **9**A is a schematic diagram showing a test process for testing the mixed signal device by the conventional semiconductor test system and FIG. **9**B is a schematic diagram showing a test process for testing the mixed signal device by the semiconductor test system of the present invention.

FIG. **10** is a schematic diagram showing an example of outward appearance of the semiconductor test system of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

The embodiment of the present invention is explained with reference to FIGS. **4**–**10**. FIG. **4** is a block diagram showing a basic structure of the semiconductor test system of the, present invention for testing an analog/digital mixed signal integrated circuit (mixed signal IC). In the semiconductor test system of the present invention, a test head (tester main frame) is so configured that one or more modular testers (hereinafter "tester module") are selectively installed therein. The tester modules to be installed can be a plurality of same tester modules depending on the number of tester pins desired or a combination of different tester modules such as a high speed module HSM and a low speed module LSM.

As will be explained with reference to FIGS. **6** and **7** later, each tester module is provided with a plurality of event tester boards **43**, for example, eight (8) tester boards. Further, each event tester board includes a plurality of event testers **66** corresponding to a plurality of tester pins, such as 32 event tester for 32 tester pins. Therefore, in the example of FIG. **4**, an event tester board $\mathbf{43}_1$ deals with an analog part of the device test while other event tester boards **43** cover a digital part of the device test.

In the test system of FIG. **4**, the plurality of event tester boards **43** are controlled by a tester controller **41**, which is a host computer of the test system, through a system bus **64**. As noted above, for example, eight event tester boards **43** may be installed in one tester module. Although not shown in FIG. **4**, typically, a test system of the present invention is configured by two or more such tester modules as shown in FIG. **6**.

In the test system of FIG. **4**, the event tester board **43** applies a test pattern (test signal) to a device under test **19**, and examines a response signal from the device under test resultant from the test pattern. For testing the analog function of the device under test, an optional circuit **48** may be provided in the test system. Such an optional circuit **48** includes, for example, a DA converter, an AD converter and a filter.

Each event tester board **43** includes event testers $\mathbf{66}_1$–$\mathbf{66}_{32}$ for 32 channels for example, an interface **53**, a processor **67** and a memory **68**. Each event tester **66** corresponds to a tester pin, and has the same inner structure within the same tester board. In this example, the event tester **66** includes an event memory **60**, an event execution unit **47**, a driver/comparator **61** and a test result memory **57**.

The event memory **60** stores event data for producing a test pattern. The event execution unit **47** produces the test pattern based on the event data from the event memory **60**. The test pattern is supplied to the device under test through the driver/comparator **61**. In the case where an input pin of the device under test is an analog input, the optional circuit **48** noted above converts the test pattern to an analog signal by the DA converter therein. Thus, the analog test signal is applied to the device under test. An output signal of the device under test is compared with an expected signal by the driver/comparator **61**, the result of which is stored in the test result memory **57**. In the case where an output signal from the device under test is an analog signal, if necessary, such an analog signal is converted to a digital signal by the AD converter in the optional circuit **48**.

FIG. **5** is a block diagram showing an example of configuration in the event tester **66** in the event tester board **43** in more detail. The further detailed description regarding the event based test system is given in the above U.S. patent application as well as U.S. patent application Ser. No. 09/259,401 owned by the same assignee of this invention. In FIG. **5**, the blocks identical to that of FIG. **4** are denoted by the same reference labels.

The interface **53** and the processor **67** are connected to the tester processor (host computer) **41** through the system bus **64**. The interface **53** is used, for example, for transferring data from the tester controller **41** to a register (not shown) in the event tester board to assign the event testers to the input/output pins of the device under test. For example, when the host computer sends a group assigning address to the system bus, the interface **53** interprets the group assigning address and allows the data from the host computer to be stored in the register in the specified event tester board.

The processor **67** is provided, for example, in each event tester board, and controls the operations in the event tester board including generation of events (test patterns), evaluation of output signals from the device under test, and acquisition of failure data. The processor **67** can be provided at each tester board or every several tester boards. Further, the processor **67** may not always necessary be provided in the event tester board, but the same control functions can be made directly by the tester controller **41** to the event tester boards.

An address controller **58** is, for example, in the most simple case, a program counter. The address controller **58** controls the address supplied to the failure data memory **57** and the event memory **60**. The event timing data is transferred to the event memory **60** from the host computer as a test program and stored therein.

The event memory **60** stores the event timing data as noted above which defines timing of each of the events (change points from "1" to "0" and from "0" to "1"). For example, the event timing data is stored as two types of data, one of which shows integer multiples of a reference clock cycle while the other shows fractions of the reference clock cycle. Preferably, the event timing data is compressed before being stored in the event memory **60**.

In the example of FIG. **5**, the event execution unit **47** in FIG. **4** is configured with a decompression unit **62**, a timing count/scaling logic **63**, and an event generator **64**. The decompression unit **62** decompresses (reproduces) the compressed timing data from the event memory **60**. The timing count/scaling logic **63** produces time length data of each event by summing or modifying the event timing data. The time length data expresses the timing of each event by a time length (delay time) from a predetermined reference point.

The event generator **64** produces a test pattern based on the time length data and provides the test pattern to the device under test **19** through the driver/comparator **61**. Thus, a particular pin of the device under test **19** is tested by evaluating the response output therefrom. The driver/comparator **61** is mainly formed with, as shown in FIG. **4**, a driver which drives the test pattern to be applied to the particular device pin and a comparator which determines a voltage level of an output signal of a device pin resultant from the test pattern and compares the output signal with the expected logic data.

In the event tester summarized above, the input signal applied to the device under test and the expected signal compared with the output signal of the device under test are produced by the data in the event based format. In the event based format, the information of change points on the input signal and expected signal is formed of action information (set and/or reset) and time information (time length from a specified point).

As noted above, in the conventional semiconductor test system, the cycle based method has been used, which requires memory capacity smaller than that required in the event based architecture. In the cycle based test system, the time information of the input signal and expected signal is formed of cycle information (rate signal) and delay time information. The action information of the input signal and expected signal is formed of waveform mode data and pattern data. In this arrangement, the delay time information can be defined only by the limited number of data. Further, to generate the pattern data with flexibility, the test program must includes many loops and/or subroutines therein. Therefore, the conventional test system requires complicated structures and operational procedures.

In the event based test system, such complicated structures and operational procedures of the conventional cycle based test system are unnecessary, thereby easily increasing the number of test pins and/or incorporating the test pins of different performances in the same test system. Although the event based test system requires a memory of large capacity, such an increase in the memory capacity is not a major problem since the increase in the memory density and the decrease in the memory cost are rapidly and continuously realized today.

As in the foregoing, in the event based test system, each of the test pins or each group of test pins can independently perform a test operation from the other. Consequently, in the case where a plurality of different kinds of test have to be performed, such as in testing the mixed signal device under test which includes an analog signal and a digital signal, such different kinds of test can be conducted in parallel at the same time. Further, start and end timings of such different kinds of test can be independently established.

FIG. **6** is a schematic diagram for establishing a semiconductor test system having test pins grouped into different performances by incorporating a plurality of tester modules of the present invention.

A test head **124** is provided with a plurality of tester modules depending on, for example, the number of pins of a test fixture **127**, a type of the device to be tested, and the number of pins of the device to be tested. As will be described later, an interface (connection) specification between the test fixture and the test module is standardized so that any tester modules can be installed in any positions in the test head.

The test fixture **127** includes a large number of elastic connectors such as pogo-pins to electrically and mechanically connect the tester modules and a performance board **128**. The device under test **19** is inserted in a test socket on the performance board **128**, thereby establishing an electrical communication with the semiconductor test system. The optional circuit **48** shown in FIG. **4** to be used in analog testing can be formed on the performance board **128** depending on the specification of the device to be tested.

Each of the tester module has a predetermined number of pin groups. For example, one high speed module HSM installs printed circuit boards corresponding to **128** test pins (test channels) while one low speed module LSM installs printed circuit boards corresponding to 256 test pins. These numbers are disclosed only for an exemplary purpose, and various other numbers of test pins are also possible. In the example of FIG. **7**, the tester module is configured by 256 channels as a basic unit in which eight (8) event tester boards **43** are installed. Each event tester board includes, for example, 32 event testers (test channels) .

As noted above, each board in the tester module has event testers each of which generates and applies test patterns to the corresponding pin of the device under test through the performance board **128**. Output signals of the device under test **19** responsive to the test pattern are transmitted to the event tester board in the tester module through the performance board **128** and are compared with the expected signals to determine the pass/fail of the device under test.

Each tester module is provided with an interface (connector) **126**. The connector **126** is so arranged to fit to the standard specification of the test fixture **127**. For example, in the standard specification of the test fixture **127**, a structure of connector pins, impedance of the pins, distance between the pins (pin pitch), and relative positions of the pins are specified for the intended test head. By using the interface (connector) **126** which matches the standard specification on all of the tester modules, test systems of various combinations of the tester modules can be freely established.

Because of the configuration of the present invention, a test system of optimum cost/performance which matches the device under test can be established. Further, improvement

of the performance of the test system can be achieved by replacing one or more test modules, thus, an overall life time of the test system can be increased. Moreover, the test system of the present invention can accommodate a plurality of test modules whose performances are different from the other, and thus, the desired performance of the test system can be achieve directly by the corresponding test module. Therefore, the performance of the test system can be easily and directly improved.

FIG. **8** is a block diagram showing a basic concept for conducting different types of test in parallel for a mixed signal device **19** having analog and digital functions by the semiconductor test system of the present invention. In this example, the mixed signal device **19** includes an AD converter circuit, a logic circuit, and a DA converter circuit. The semiconductor test system of the present invention can perform test for each group of specified number of tester pins independently from the other group as noted above. Therefore, by assigning the groups of tester pins to these circuits in the mixed signal device, these circuits can be tested in parallel at the same time.

FIG. **9**A is a schematic diagram showing a test process for testing the mixed signal device by the conventional semiconductor test system and FIG. **9**B is a schematic diagram showing a test process for testing the mixed signal device by the semiconductor test system of the present invention. When testing the mixed signal IC having analog and digital circuits such as shown in FIG. **8** by the conventional semiconductor test system, the test must proceed in a series fashion such as completing one test and moving to the next test. Therefore, the overall time required for completing the test is the sum of times of all of the tests as shown in FIG. **9**A.

In contrast, when testing the mixed signal IC shown in FIG. **8** by the semiconductor test system of the present invention, the AD converter circuit, logic circuit and DA converter circuit can be tested in parallel at the same time as shown in FIG. **9**B. Thus, the present invention can dramatically reduce the overall test time. Since it is a common practice to evaluate the test result of the AD converter circuit or DA converter circuit by predetermined formulas, a computation time after each of the AD and DA circuit test is provided in FIGS. **9**A and **9**B.

An example of outer appearance of the semiconductor test system of the present invention is shown in the schematic diagram of FIG. **10**. In FIG. **10**, a host computer (main system computer) **41** is, for example, a work station having a graphic user interface (GUI). The host computer functions as a user interface as well as a controller to control an overall operation of the test system. The host computer **41** and the inner hardware of the test system are connected through the system bus **64** (FIGS. **4** and **5**).

The event based test system of the present invention does not need the pattern generator and the timing generator used in the conventional semiconductor test system configured by the cycle based concept. Therefore, it is possible to substantially decrease the physical size of the overall test system by installing all of the modular event testers in the test head (or tester main frame) **124**.

As has been foregoing, in the event based semiconductor test system of the present invention, each test pin can operate independently from the other test pins. Thus, by assigning groups of test pins to different devices or blocks under test, two or more different devices or blocks can be tested at the same time. Therefore, according to the semiconductor test system of the present invention, an analog circuit and a digital circuit in a mixed signal device can be tested in parallel at the same time.

As noted above, in the semiconductor test system of the present invention, the tester module (tester board) is configured by event based architecture where all the information required for executing the test is prepared in the event based format. Therefore, the rate signal showing the start timing of each test cycle or the pattern generator which operates in synchronism with the rate signal used in the conventional technology are no longer necessary. Because it is not necessary to include the rate signal or pattern generator, each test pin in the event based test system can operate independently from the other test pins. Therefore, different types of test, such as analog circuit test and digital circuit test can be performed at the same time.

Since the semiconductor test system of the present invention has a modular structure, a desired test system can be formed freely depending on the kind of devices to be tested and the purpose of the test. Further, the hardware of the event based test system can be dramatically reduced while the software for the test system can be dramatically simplified. Accordingly, the tester modules of different capabilities and performances can be installed together in the same test system. Furthermore, as shown in FIG. **6**, an overall physical size of the event based test system can be considerably reduced, resulting in further cost reduction, floor space reduction and associated cost savings.

Further in the semiconductor test system of the present invention, the logic simulation data in the design stage of the device in the electronic design automation (EDA) environment can be directly used to produce the test pattern to test the device in the evaluation stage. Thus, a turnaround time between the design of the device and the evaluation of the device can be substantially decreased, thereby further decreasing the test cost while increasing the test efficiency.

What is claimed is:

1. A semiconductor test system for testing a mixed signal integrated circuit, comprising:

two or more tester modules whose performances are different from one another where each tester module includes at least one event tester which produces a test pattern based on test data described in an event format;

a test head to accommodate the two or more tester modules having different performances;

means provided on the test head for electrically connecting the tester modules and a device under test;

an optional circuit corresponding to the device under test when the device under test is a mixed signal integrated circuit having an analog function block and a digital function block, and

a host computer for controlling an overall operation of the test system by communicating with the tester modules through a tester bus;

whereby the analog function block and the digital function block of the mixed signal integrated circuit being tested in parallel at the same time, and wherein the

event data defines events as any changes in the test pattern generated by the event tester at timings relative to one fixed reference point.

2. A semiconductor test system for testing a mixed signal integrated circuit as defined in claim 1, wherein one type of the performances of the tester module is a high speed and high timing resolution while another type of performance is a low speed and low timing resolution.

3. A semiconductor test system for testing a mixed signal integrated circuit as defined in claim 1, wherein interface specification for connecting the tester modules and the means for electrically connecting the tester modules and the device under test is standardized.

4. A semiconductor test system for testing a mixed signal integrated circuit as defined in claim 1, wherein the means for electrically connecting the tester modules and the device under test is comprised of a performance board having a test socket for mounting the device under test thereon and signal patterns connected to the test socket, and a test fixture having a connection mechanism for electrically connecting between the performance board and the tester modules, thereby establishing electrical communication between the device under test and the tester modules.

5. A semiconductor test system for testing a mixed signal integrated circuit as defined in claim 1, wherein a number of tester pins for each tester module is variable.

6. A semiconductor test system for testing a mixed signal integrated circuit as defined in claim 1, wherein a number of tester pins is variably assigned to the tester module, and such assignment of test pins and modification thereof are regulated by address data from the host computer.

7. A semiconductor test system for testing a mixed signal integrated circuit as defined in claim 1, wherein each of the tester modules includes a plurality of event tester boards where each of the event tester boards includes a plurality of event testers which are assigned to a predetermined number of test pins.

8. A semiconductor test system for testing a mixed signal integrated circuit as defined in claim 7, wherein each of the tester modules corresponds to one of the event tester boards.

9. A semiconductor test system for testing a mixed signal integrated circuit as defined in claim 7, wherein each of the tester modules includes a plurality of event tester boards wherein each of the event tester boards includes an inner controller where the inner controller controls, in response to instructions from the host computer, to generate a test pattern, supply the test pattern to the device under test, and to evaluate an output signal of the device under test.

10. A semiconductor test system for testing a mixed signal integrated circuit as defined in claim 1, wherein each of the tester modules includes an inner controller where the inner controller controls, in response to instructions from the host computer, to generate a test pattern from the tester module, supply the test pattern to the device under test, and to evaluate an output signal of the device under test.

11. A semiconductor test system for testing a mixed signal integrated circuit as defined in claim 1, wherein each of the tester modules includes a plurality of event tester boards each having a plurality of event tester where each of the event testers is assigned to one test pin, wherein each event tester is comprised of:

a controller which controls, in response to instructions from the host computer, an operation of the event tester;

an event memory for storing timing data for each event;

an address sequencer for providing, under the control of the controller, address data to the event memory;

means for producing the test pattern based on the timing data from the event memory; and

a driver/comparator for transferring the test pattern to a corresponding pin of the device under test and receiving the output signal from the device under test.

* * * * *

DAC & ADC
Up to 32 sites

US006449741B1

(12) **United States Patent**
Organ et al.

(10) **Patent No.: US 6,449,741 B1**
(45) **Date of Patent: *Sep. 10, 2002**

(54) **SINGLE PLATFORM ELECTRONIC TESTER**

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(73) Assignee: **LTX Corporation**, Westwood, MA (US)

(*) Notice: This patent issued on a continued prosecution application filed under 37 CFR 1.53(d), and is subject to the twenty year patent term provisions of 35 U.S.C. 154(a)(2).

Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **09/183,038**

(22) Filed: **Oct. 30, 1998**

(51) **Int. Cl.**[7] **H02H 3/05**; G01R 31/28

(52) **U.S. Cl.** **714/724**; 714/46

(58) **Field of Search** 714/724, 725, 714/733, 734, 735, 736, 737, 738, 739, 25, 26, 30, 31, 32, 37, 44, 46, 47, 57; 324/763, 764, 758.1, 73.1, 537, 750

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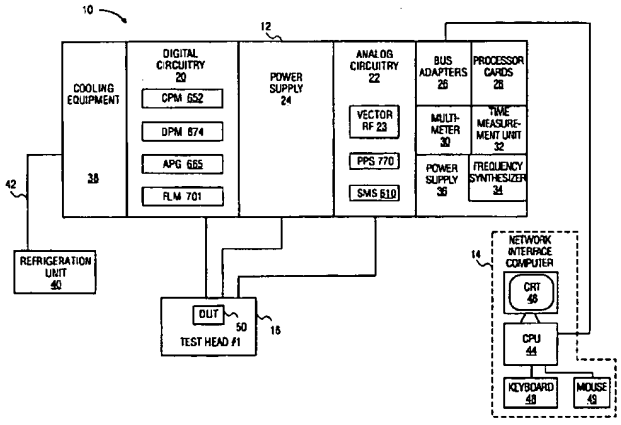
Primary Examiner—Christine T. Tu
(74) *Attorney, Agent, or Firm*—Blakely, Sokoloff, Taylor & Zafman LLP

(57) **ABSTRACT**

An electronic tester with digital, and analog, and memory test circuitry on a single platform. A test head is coupled to a device under test. The device under test can be a system-on-a-chip integrated circuit, a mixed signal integrated circuit, a digital integrated circuit, or an analog integrated circuit. Digital test circuitry applies digital test signals to the device under test coupled to the test head and receives digital outputs from the device under test in response to the digital test signals. Analog test circuitry applies analog test signals to the device under test coupled to the test head and receives analog outputs from the device under test in response to the analog test signals. Memory test circuitry applies memory test patterns to the device under test coupled to the test head and receives memory outputs from the device under test in response to the memory test patterns. A tester computer supervises the application of digital, analog, and memory test signals from the digital, analog, and memory test circuitry to the device under test such that signals applied to the device under test can be solely digital test signals, solely analog test signals, solely memory test signals, or mixed digital, analog, and memory test signals. The test head, the digital test circuitry, the analog test circuitry, the memory test circuitry, and the computer are operable as a single platform.

11 Claims, 26 Drawing Sheets



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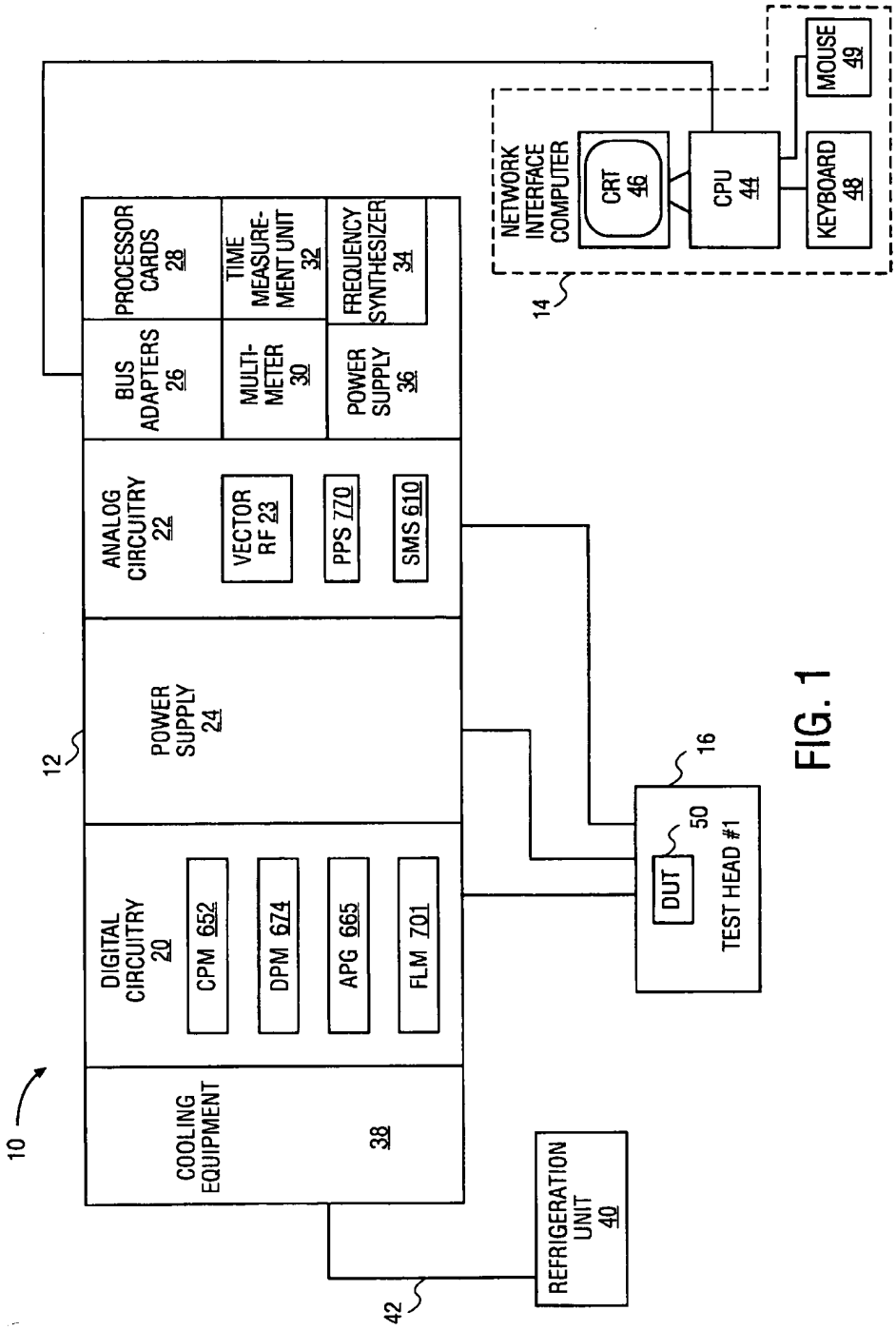
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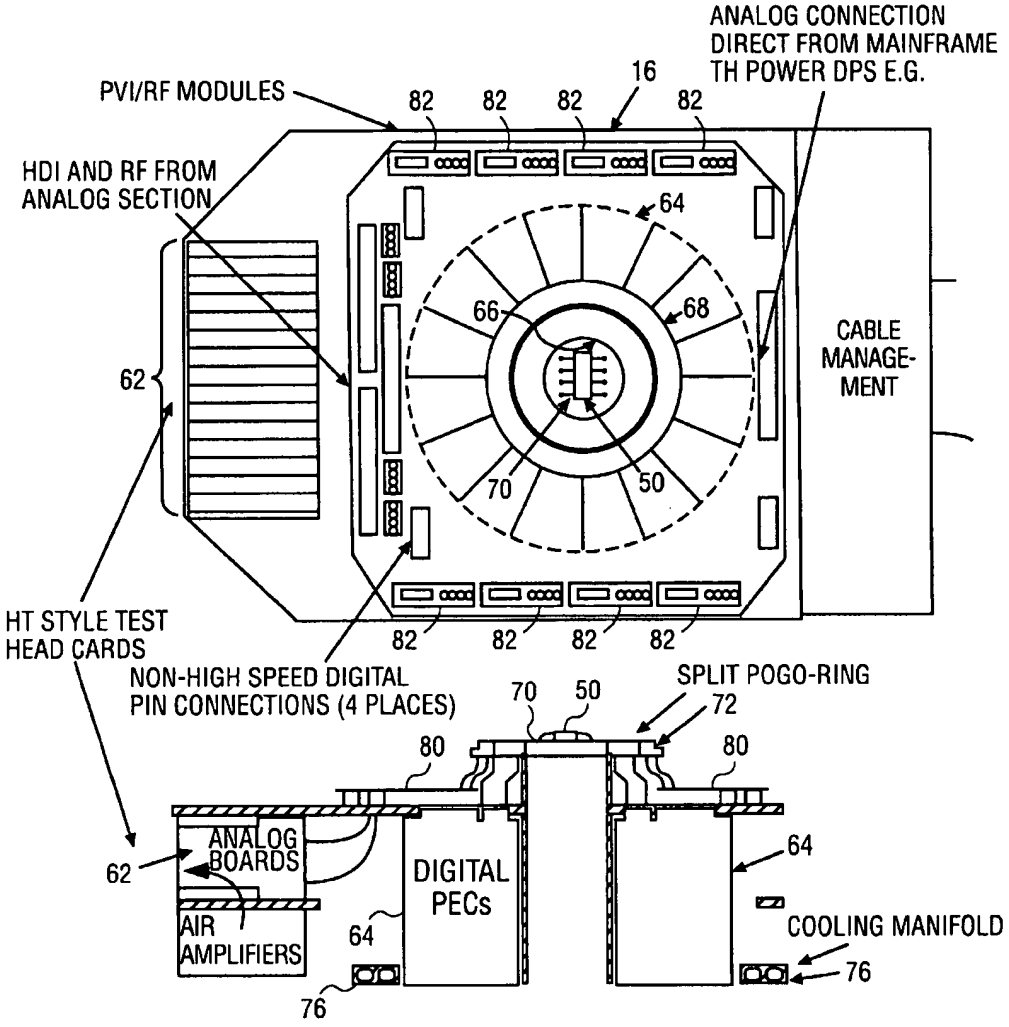
DIGITAL CIRCUITRY 20
CPM 652
DPM 674
APG 665
FLM 701
POWER SUPPLY 24
ANALOG CIRCUITRY 22
VECTOR RF 23
PPS 770
SMS 610
BUS ADAPTERS 26
MULTI-METER 30
POWER SUPPLY 36
PROCESSOR CARDS 28
TIME MEASURE-MENT UNIT 32
FREQUENCY SYNTHESIZER 34
NETWORK INTERFACE COMPUTER
CRT 46
CPU 44
KEYBOARD 48
MOUSE 49
REFRIGERATION UNIT 40
DUT
TEST HEAD #1

FIG. 1


ANALOG CONNECTION
DIRECT FROM MAINFRAME
TH POWER DPS E.G.
PVI/RF MODULES
16
82
82
82
82
HDI AND RF FROM
ANALOG SECTION
64
66
68
62
CABLE
MANAGE-
MENT
70
50
HT STYLE TEST
HEAD CARDS
82
82
82
82
NON-HIGH SPEED DIGITAL
PIN CONNECTIONS (4 PLACES)
SPLIT POGO-RING
70
50
72
80
80
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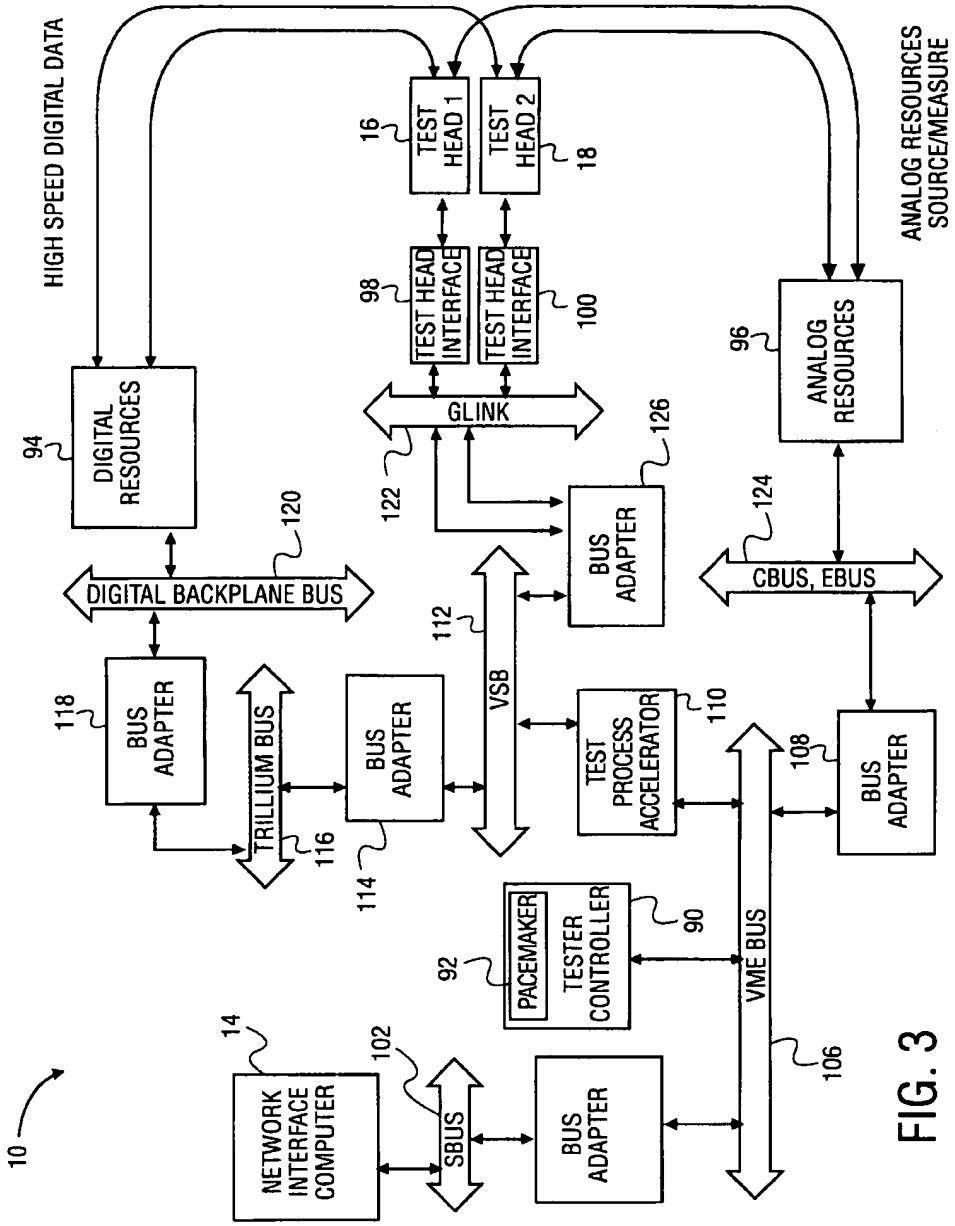
DIGITAL
PECs
64
AIR
AMPLIFIERS
64
COOLING MANIFOLD
76
76

FIG. 2


HIGH SPEED DIGITAL DATA
ANALOG RESOURCES SOURCE/MEASURE
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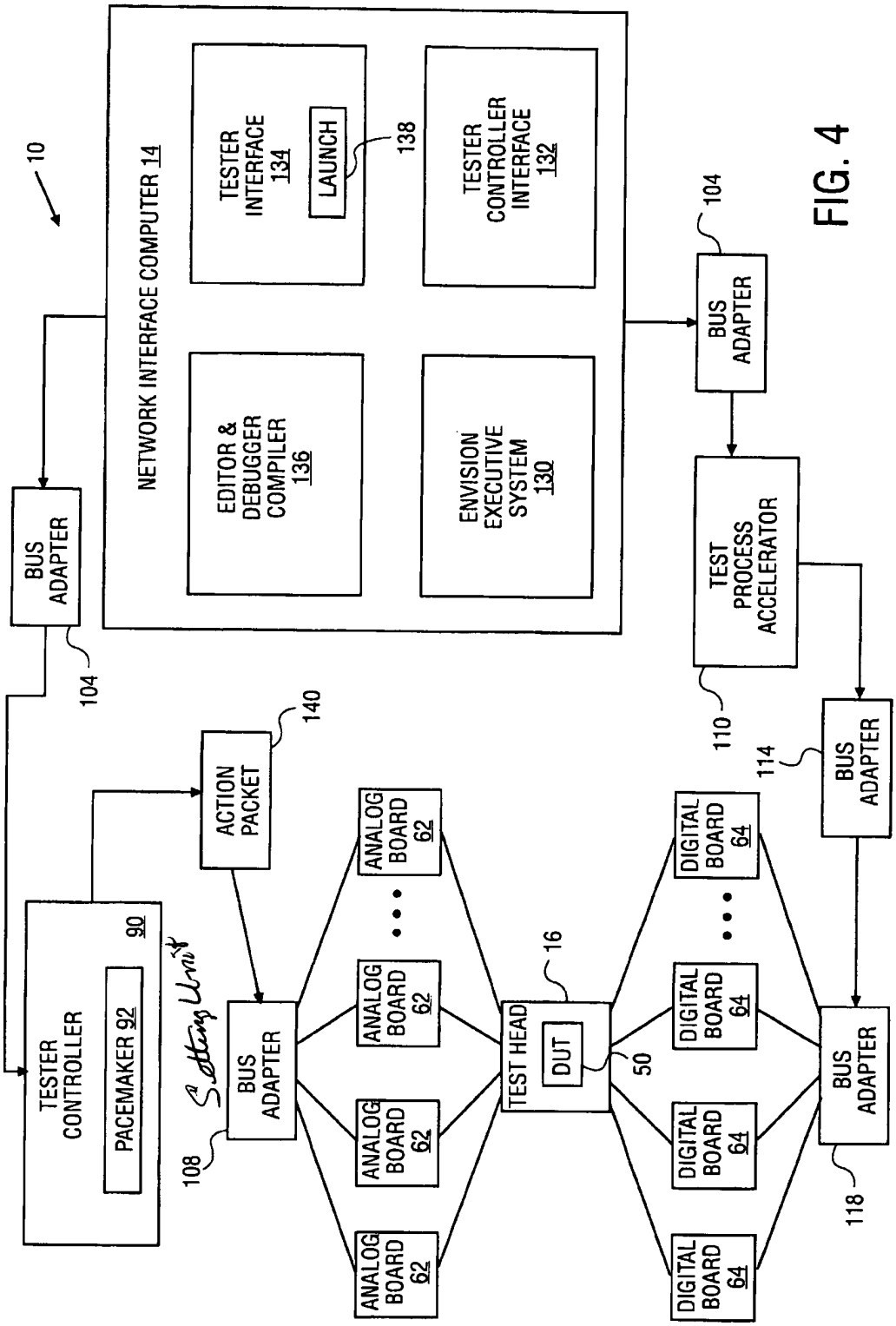
TEST HEAD 1
TEST HEAD 2
18
98
TEST HEAD INTERFACE
TEST HEAD INTERFACE
100
GLINK
122
126
94
DIGITAL RESOURCES
96
ANALOG RESOURCES
120
DIGITAL BACKPLANE BUS
BUS ADAPTER
124
CBUS, EBUS
112
VSB
118
BUS ADAPTER
TRILLIUM BUS
BUS ADAPTER
TEST PROCESS ACCELERATOR
110
108
BUS ADAPTER
116
114
PACEMAKER
TESTER CONTROLLER
90
92
VME BUS
14
102
NETWORK INTERFACE COMPUTER
SBUS
BUS ADAPTER
106
10

FIG. 3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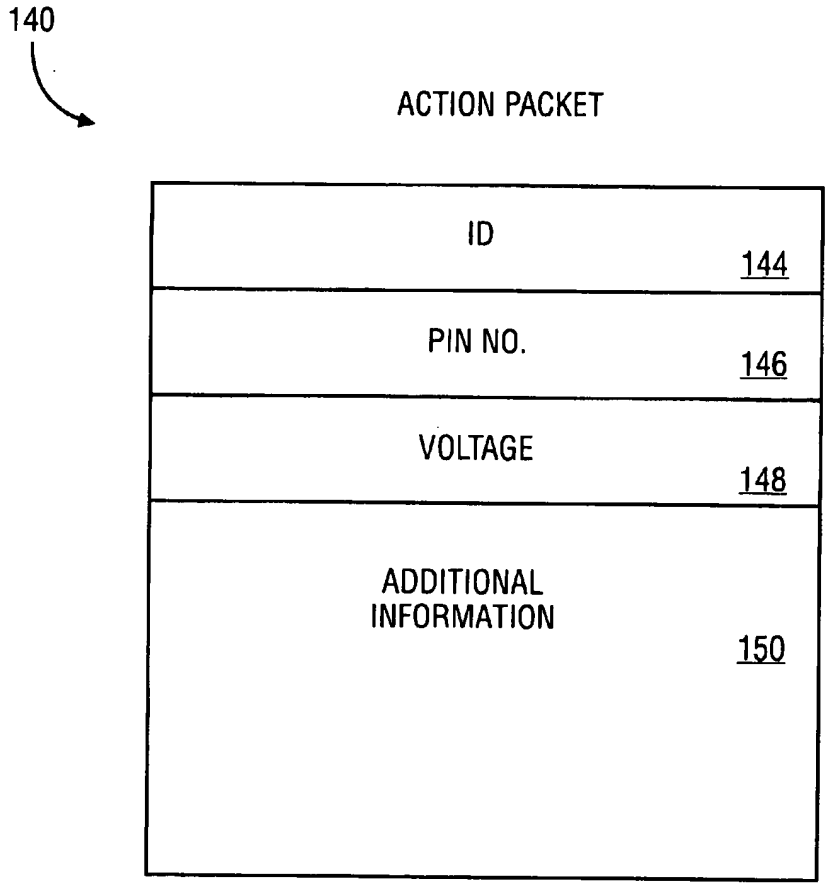
NETWORK INTERFACE COMPUTER 14
TESTER INTERFACE 134
LAUNCH
138
TESTER CONTROLLER INTERFACE 132
EDITOR & DEBUGGER COMPILER 136
ENVISION EXECUTIVE SYSTEM 130
BUS ADAPTER
104
BUS ADAPTER
104
TEST PROCESS ACCELERATOR
110
BUS ADAPTER
114
ACTION PACKET
140
TESTER CONTROLLER
PACEMAKER 92
90
BUS ADAPTER
108
ANALOG BOARD 62
ANALOG BOARD 62
ANALOG BOARD 62
TEST HEAD
DUT
16
50
DIGITAL BOARD 64
DIGITAL BOARD 64
DIGITAL BOARD 64
BUS ADAPTER
118

FIG. 4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ACTION PACKET
ID
144
PIN NO.
146
VOLTAGE
148
ADDITIONAL INFORMATION
150

FIG. 5

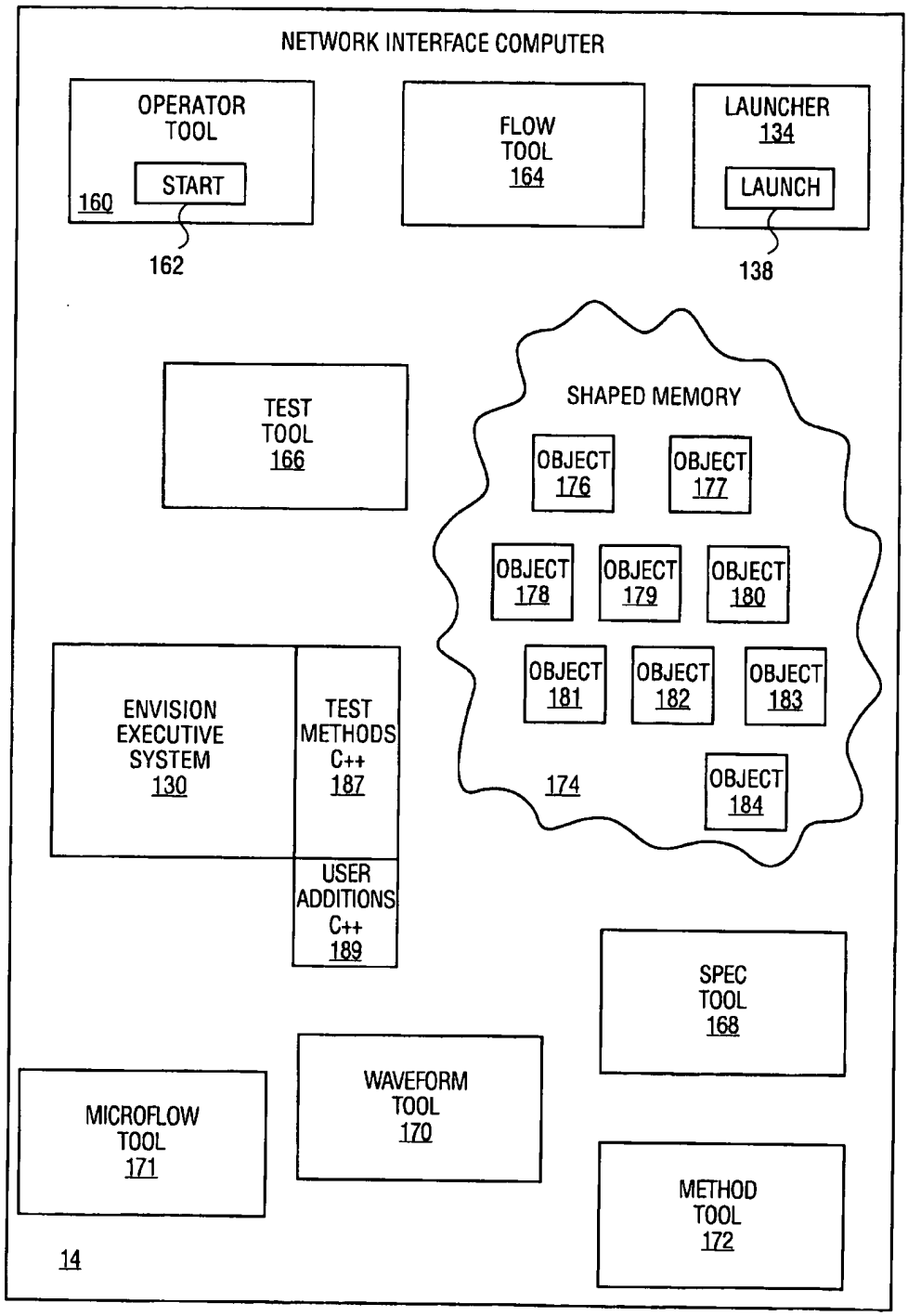

NETWORK INTERFACE COMPUTER
OPERATOR TOOL
START
160
162
FLOW TOOL 164
LAUNCHER 134
LAUNCH
138
TEST TOOL 166
SHAPED MEMORY
OBJECT 176
OBJECT 177
OBJECT 178
OBJECT 179
OBJECT 180
OBJECT 181
OBJECT 182
OBJECT 183
OBJECT 184
174
ENVISION EXECUTIVE SYSTEM 130
TEST METHODS C++ 187
USER ADDITIONS C++ 189
SPEC TOOL 168
WAVEFORM TOOL 170
MICROFLOW TOOL 171
METHOD TOOL 172
14

FIG. 6

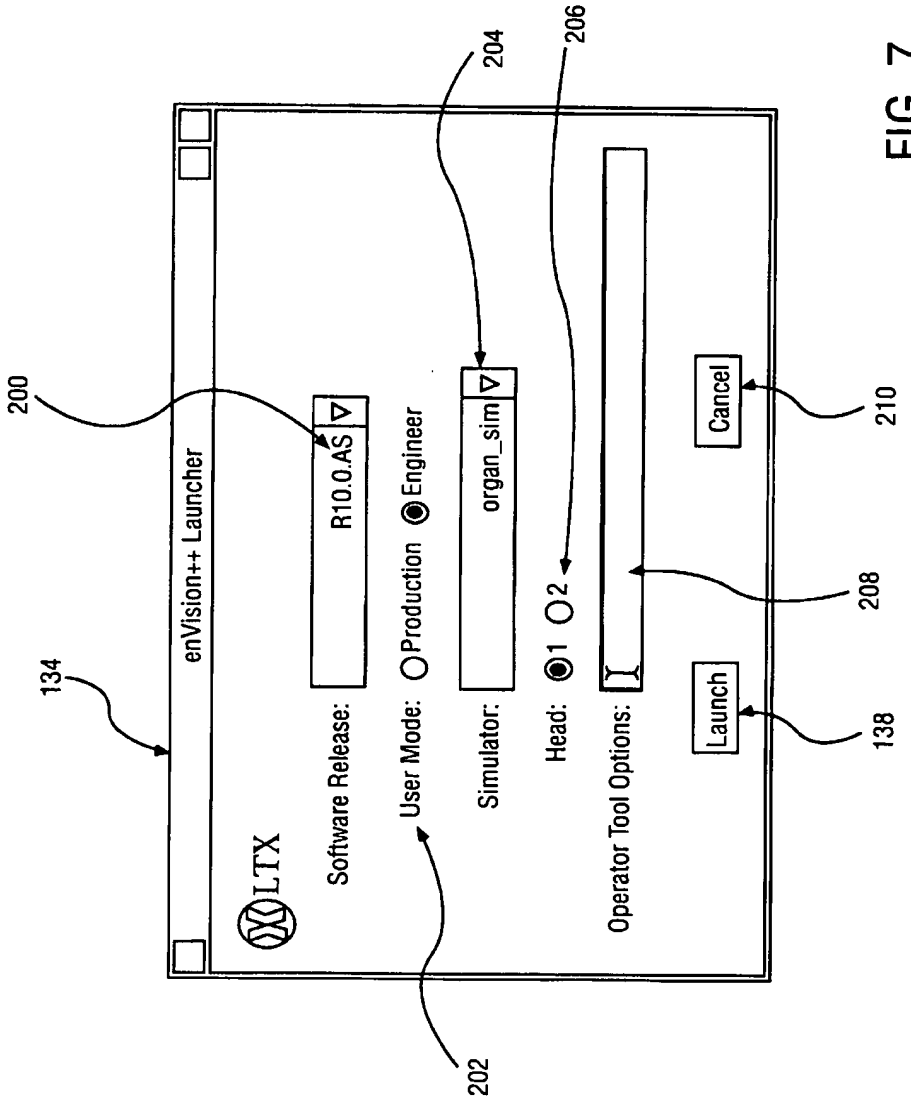
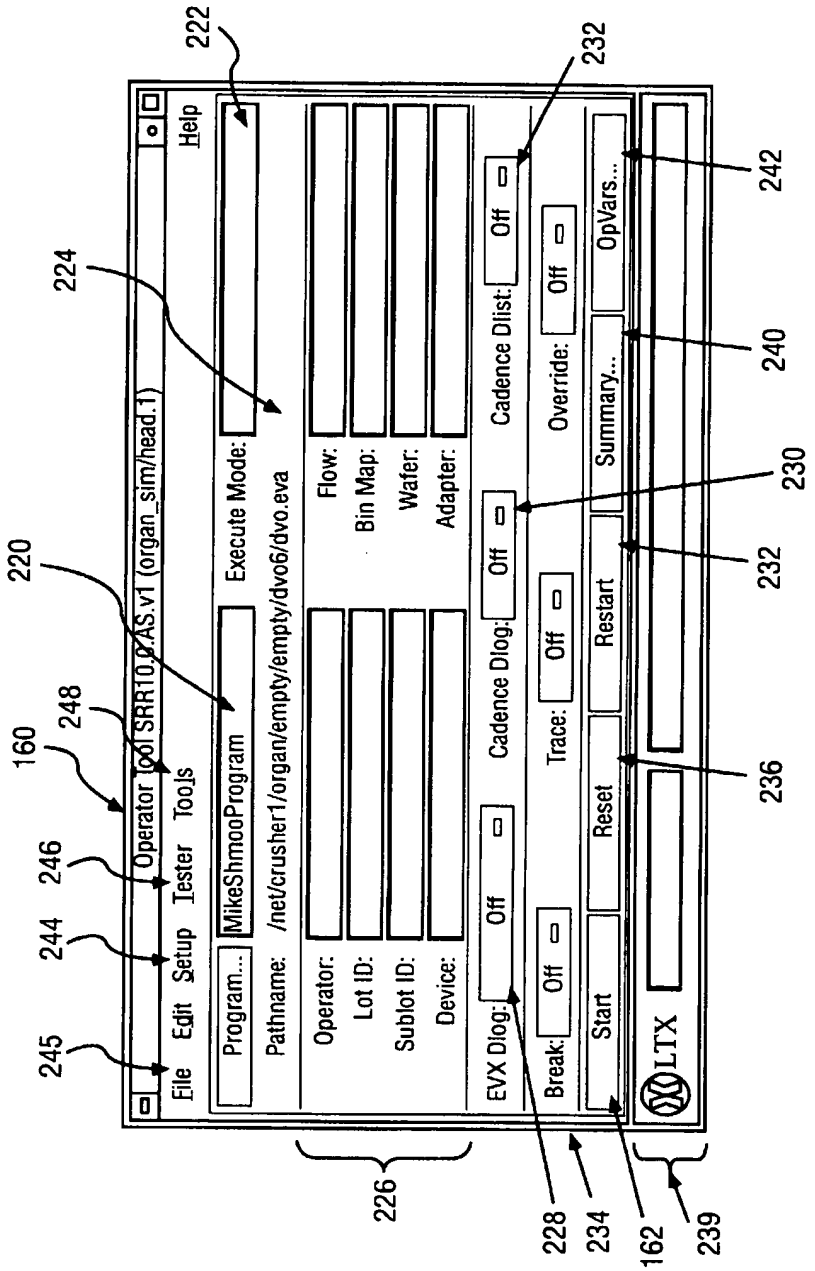

200
204
206
134
enVision++ Launcher
R10.0.AS
organ_sim
Software Release:
User Mode: Production Engineer
Simulator:
Head: 1 2
Operator Tool Options:
Cancel
Launch
208
210
138
202
LTX

FIG. 7


File Edit Setup Tester Tools Operator Help
Program...
MikeShmooProgram
Pathname: /net/crusher1/organ/empty/empty/dvo6/dvo.eva
Execute Mode:
Operator:
Lot ID:
Sublot ID:
Device:
Flow:
Bin Map:
Wafer:
Adapter:
EVX Dlog:
Off
Cadence Dlog:
Off
Break:
Off
Trace:
Off
Cadence Dlist:
Off
Override:
Off
Start
Reset
Restart
Summary...
OpVars...
LTX
222
224
220
160
248
246
244
245
226
228
234
162
239
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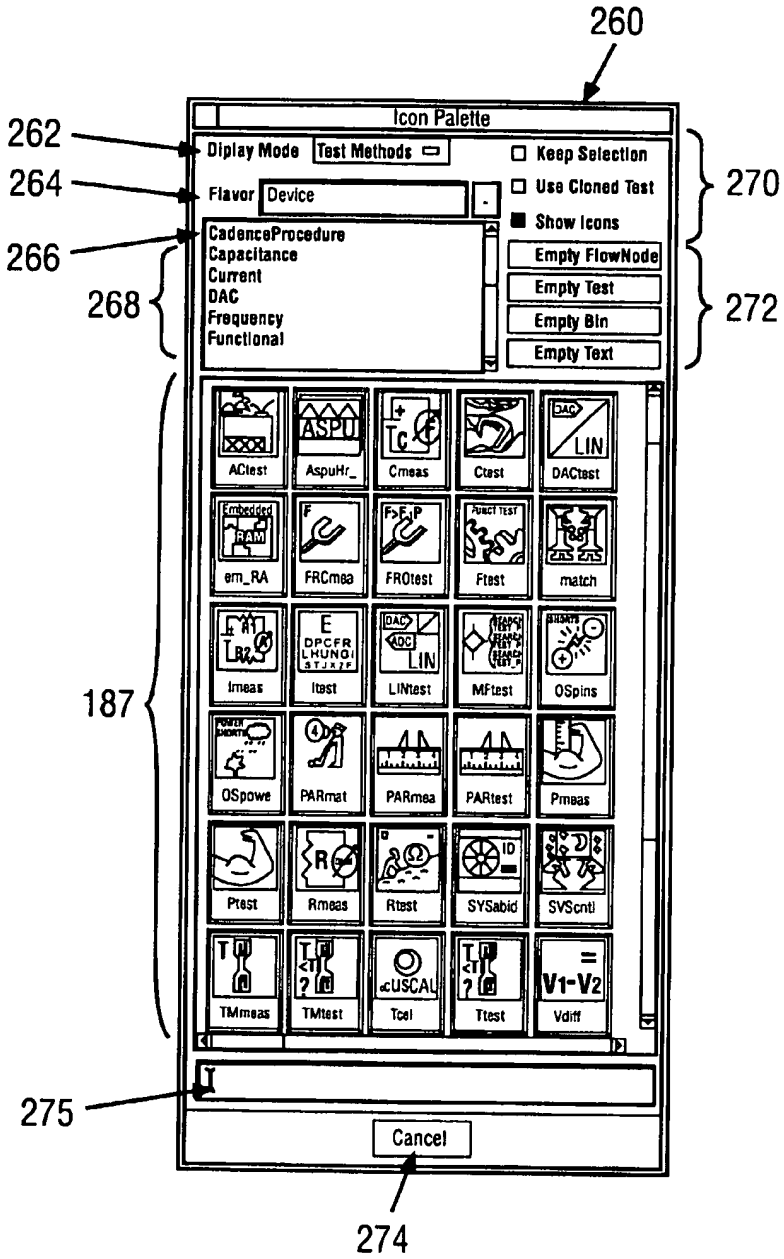
230
232
240
242
236

FIG. 8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Icon Palette
262
Diplay Mode
Test Methods
Keep Selection
264
Flavor
Device
Use Cloned Test
270
Show Icons
266
CadenceProcedure
Capacitance
Current
DAC
Frequency
Functional
Empty FlowNode
Empty Test
Empty Bin
Empty Text
268
272
187
ACtest
AspuHr_
Cmeas
Ctest
DACtest
em_RA
FRCmea
FROtest
Ftest
match
Imeas
Itest
LINtest
MFtest
OSpins
OSpowe
PARmat
PARmea
PARtest
Pmeas
Ptest
Rmeas
Rtest
SYSabid
SVScntl
TMmeas
TMtest
Tcal
Ttest
Vdiff
275
Cancel
274

FIG. 9

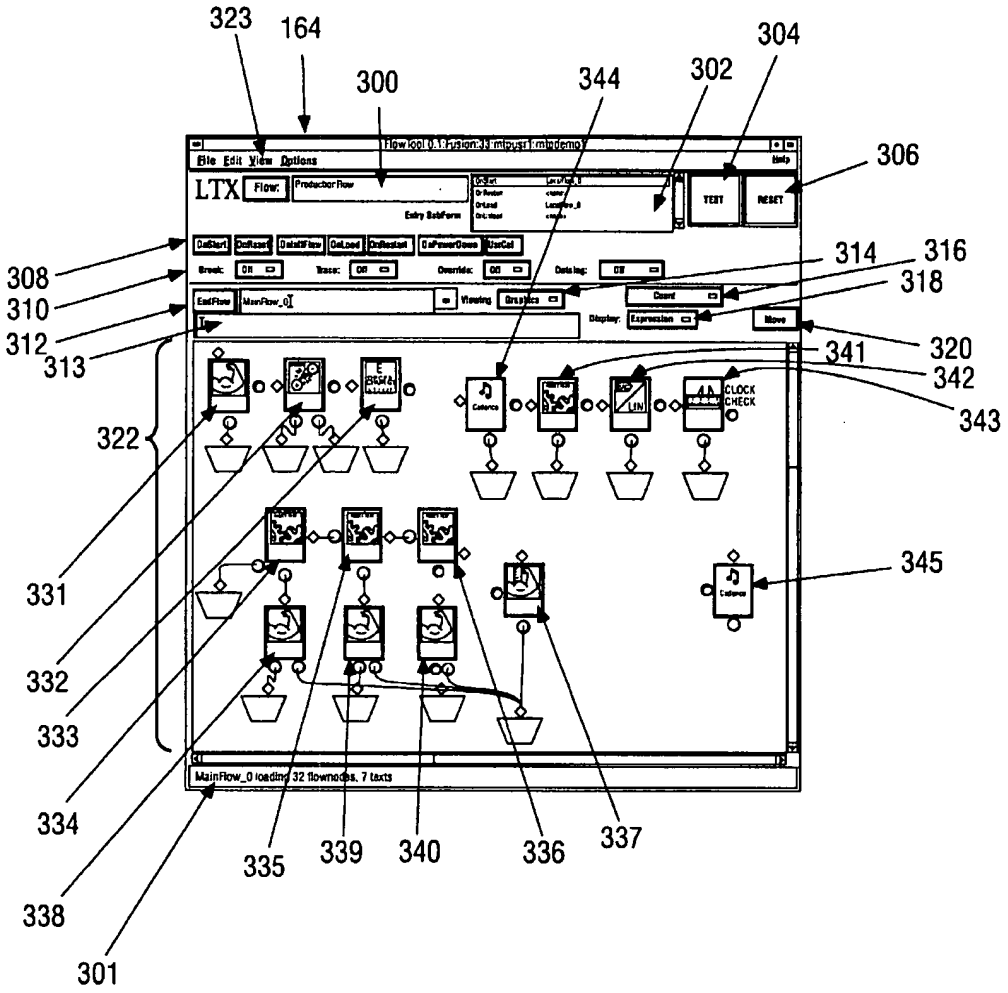
323
164
300
344
302
304
306
308
310
312
313
314
316
318
320
341
342
343
322
331
332
333
334
335
339
340
336
337
345
338
301
LTX
TEST
RESET
CLOCK CHECK

FIG. 10

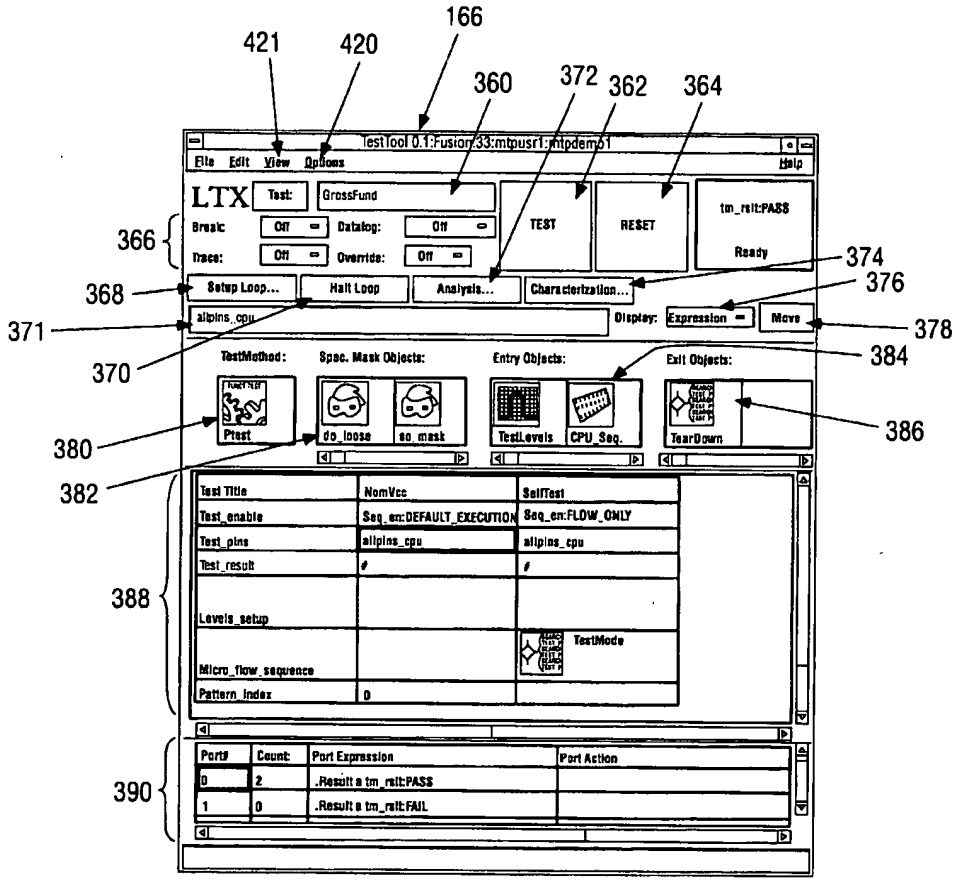
166
421
420
360
372
362
364
366
368
371
370
374
376
378
384
386
380
382
388
390
LTX
Test:
GrossFund
Break:
Trace:
Datalog:
Override:
TEST
RESET
tm_rslt:PASS
Ready
Setup Loop...
Halt Loop
Analysis...
Characterization...
allpins_cpu
Display:
Expression
Move
TestMethod:
Spec. Mask Objects:
Entry Objects:
Exit Objects:
Ptest
do_loose
so_mask
TestLevels
CPU_Seq.
TearDown
Test Title
NomVcc
SelfTest
Test_enable
Seq_en:DEFAULT_EXECUTION
Seq_en:FLOW_ONLY
Test_pins
allpins_cpu
Test_result
Levels_setup
TestMode
Micro_flow_sequence
Pattern_index
Port#
Count:
Port Expression
Port Action
.Result a tm_rslt:PASS
.Result a tm_rslt:FAIL

FIG. 11

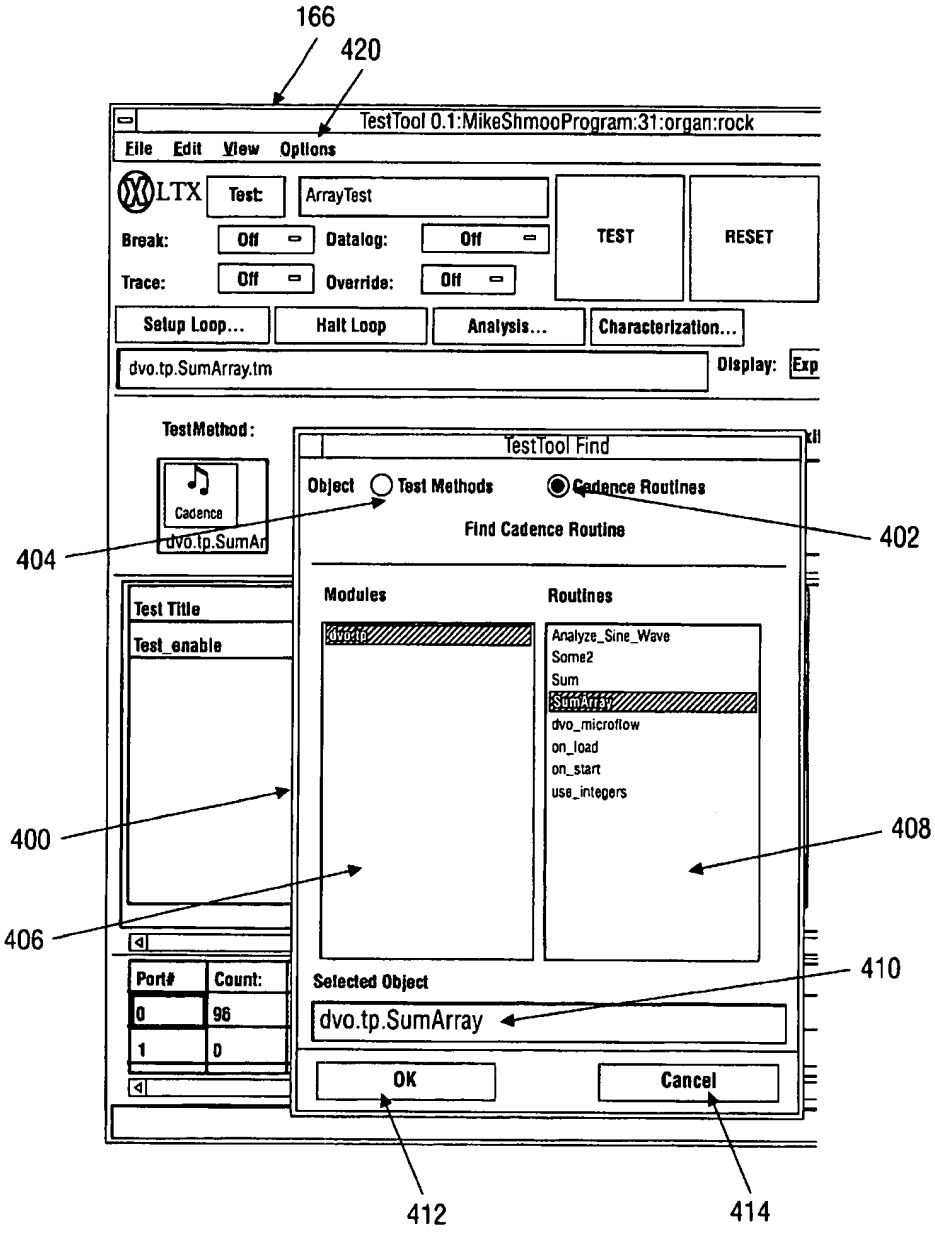
166
420
TestTool 0.1:MikeShmooProgram:31:organ:rock
File Edit View Options
LTX
Test:
ArrayTest
Break:
Off
Datalog:
Off
Trace:
Off
Override:
Off
TEST
RESET
Setup Loop...
Halt Loop
Analysis...
Characterization...
dvo.tp.SumArray.tm
Display:
Exp
TestMethod:
Cadence
dvo.tp.SumAr
TestTool Find
Object
Test Methods
Cadence Routines
Find Cadence Routine
404
402
Modules
Routines
Test Title
Test_enable
Analyze_Sine_Wave
Some2
Sum
dvo_microflow
on_load
on_start
use_integers
400
408
406
Port#
Count:
0
96
1
0
Selected Object
410
dvo.tp.SumArray
OK
Cancel
412
414

FIG. 12

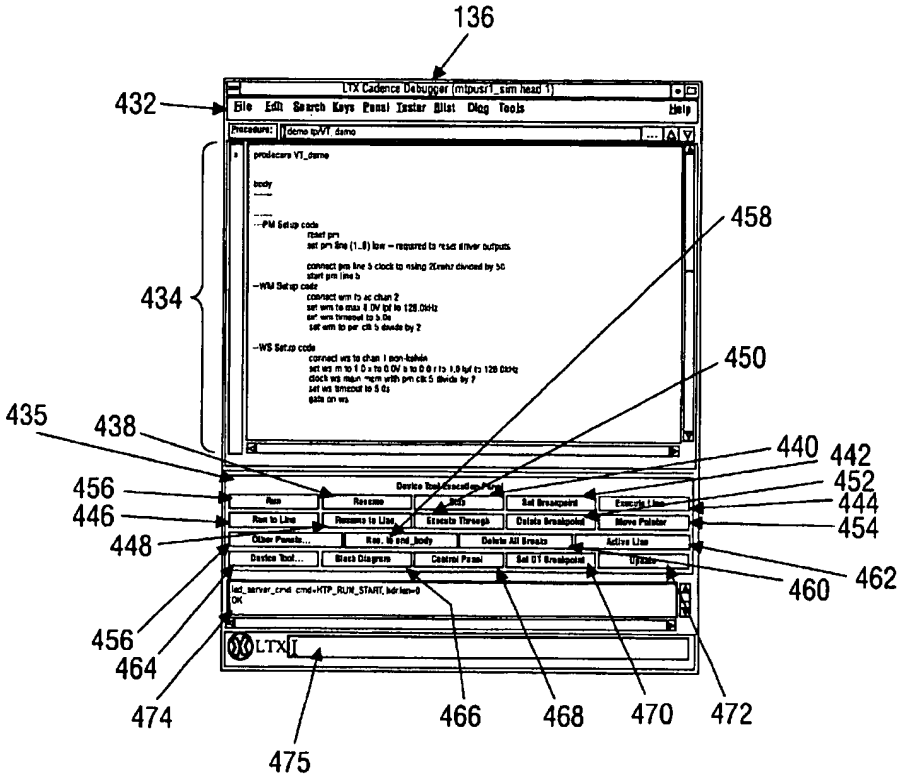
136
432
434
458
450
435
438
440
442
452
444
454
456
446
448
462
460
456
464
474
475
466
468
470
472

FIG. 13

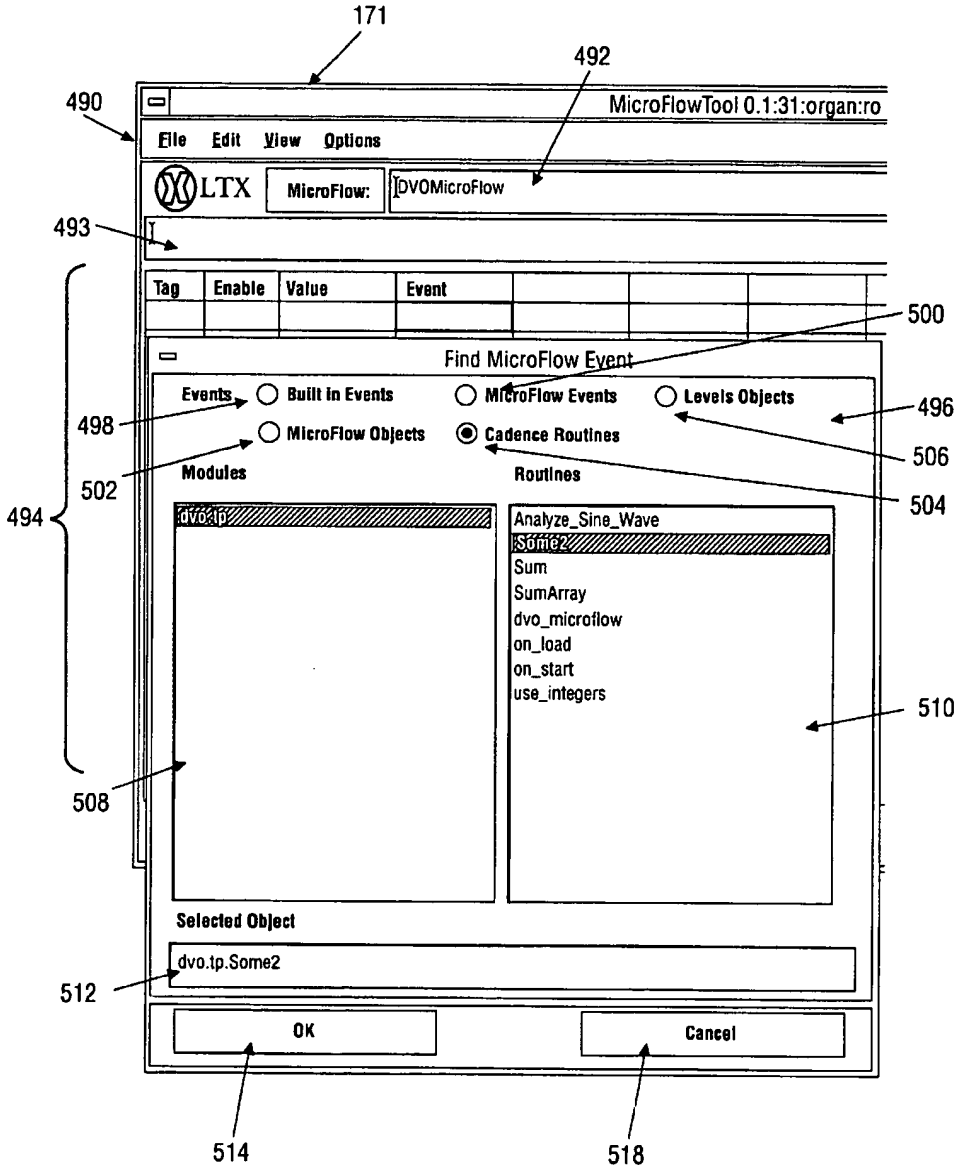
171
492
490
MicroFlowTool 0.1:31:organ:ro
File Edit View Options
LTX
MicroFlow:
DVOMicroFlow
493
Tag
Enable
Value
Event
500
Find MicroFlow Event
Events
Built In Events
MicroFlow Events
Levels Objects
496
498
MicroFlow Objects
Cadence Routines
506
Modules
Routines
502
504
494
dvo.tp
Analyze_Sine_Wave
Some2
Sum
SumArray
dvo_microflow
on_load
on_start
use_integers
510
508
Selected Object
dvo.tp.Some2
512
OK
Cancel
514
518

FIG. 14

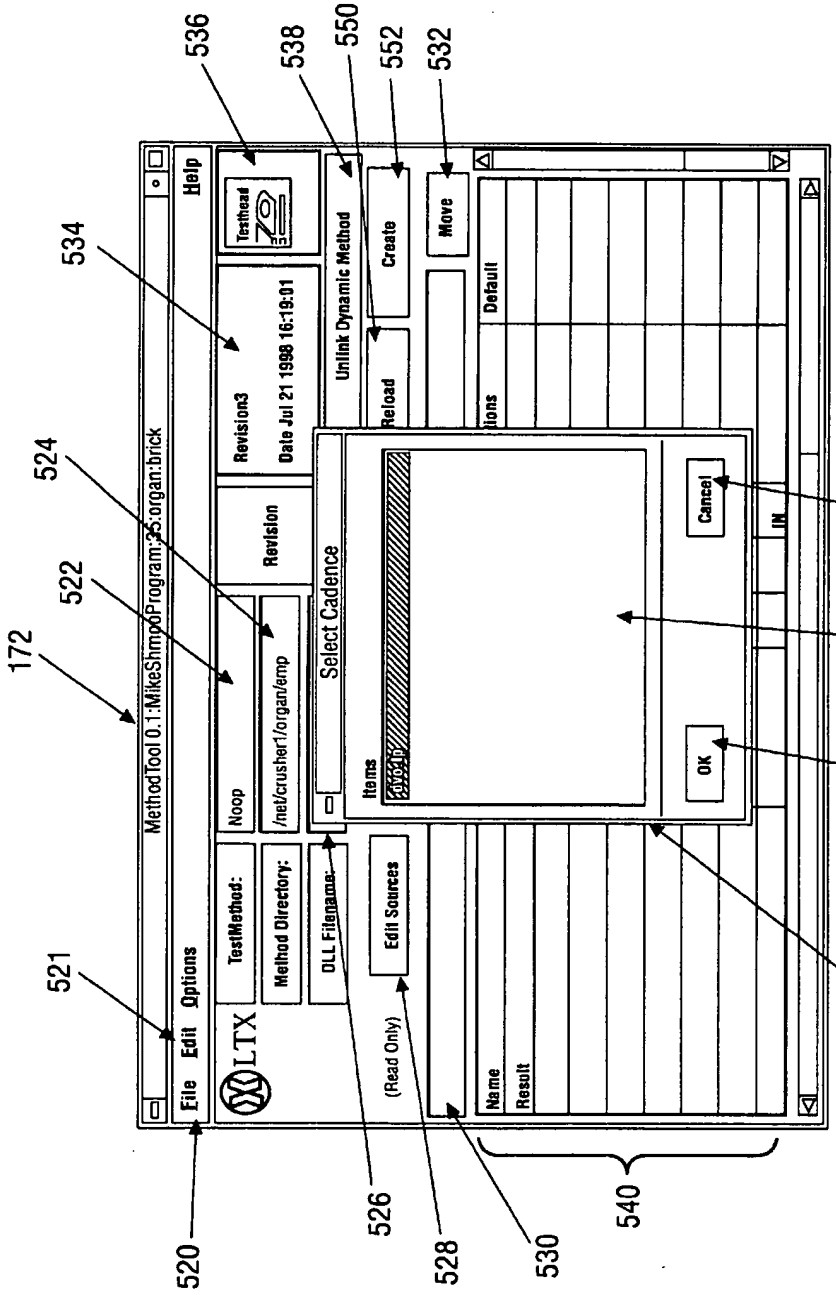
536
538
550
552
532
534
524
522
172
521
520
526
528
530
540
542
544
546
548
MethodTool 0.1:MikeShmpoProgram:25:organ:brick
File Edit Options Help
LTX
TestMethod:
Method Directory:
DLL Filename:
Noop
/net/crusher1/organ/emp
Revision
Revision3
Date Jul 21 1998 16:19:01
Testhead
Unlink Dynamic Method
Create
Move
Reload
Default
Select Cadence
Items
Cancel
OK
Edit Sources
(Read Only)
Name
Result

FIG. 15

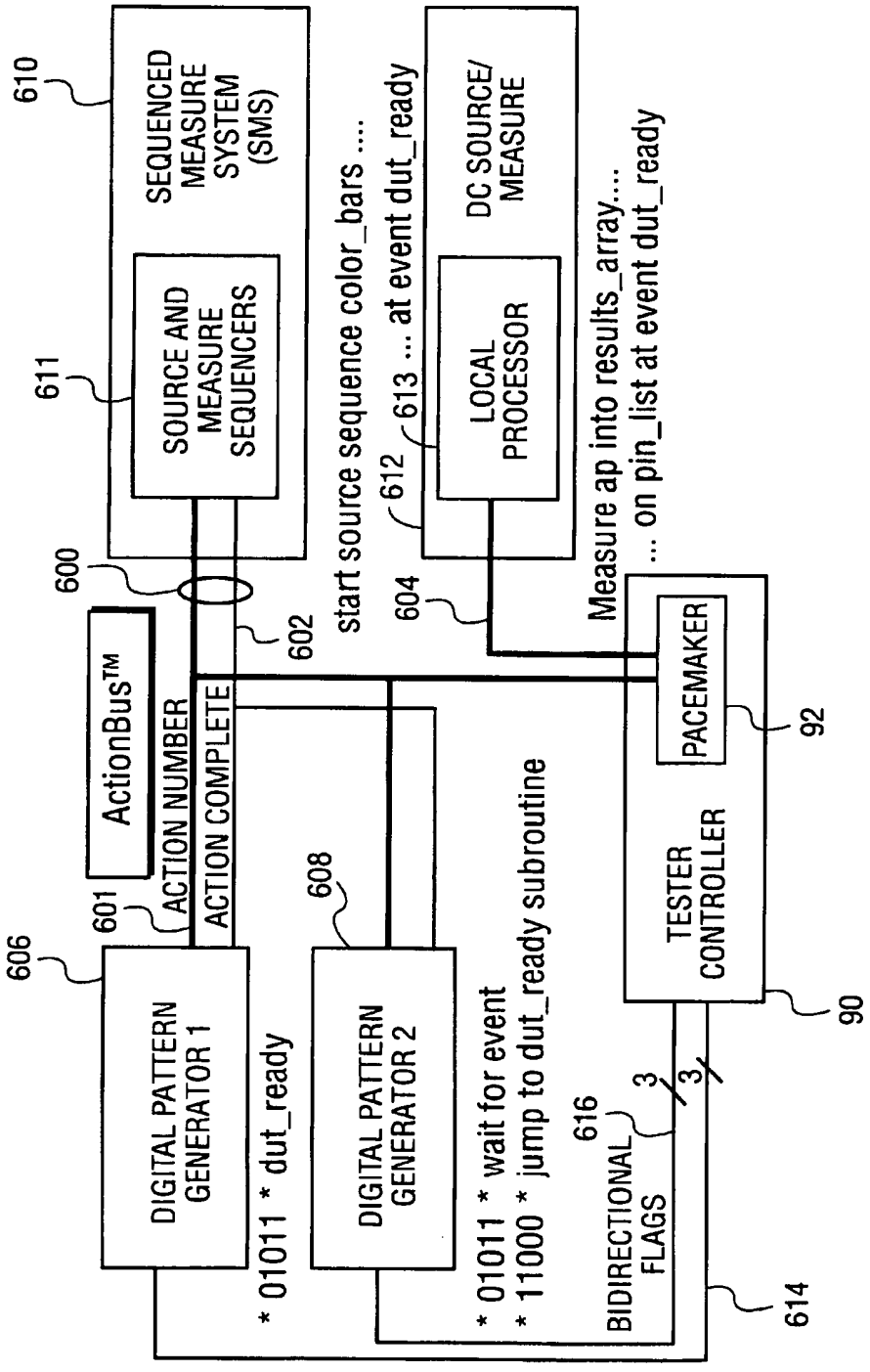
610
SEQUENCED MEASURE SYSTEM (SMS)
611
SOURCE AND MEASURE SEQUENCERS
600
ActionBus™
601
ACTION NUMBER
ACTION COMPLETE
602
start source sequence color_bars ....
612
613 ... at event dut_ready
DC SOURCE/ MEASURE
LOCAL PROCESSOR
604
Measure ap into results_array....
... on pin_list at event dut_ready
PACEMAKER
92
606
DIGITAL PATTERN GENERATOR 1
* 01011 * dut_ready
608
DIGITAL PATTERN GENERATOR 2
* 01011 * wait for event
* 11000 * jump to dut_ready subroutine
TESTER CONTROLLER
90
616
BIDIRECTIONAL FLAGS
3
3
614

FIG. 16

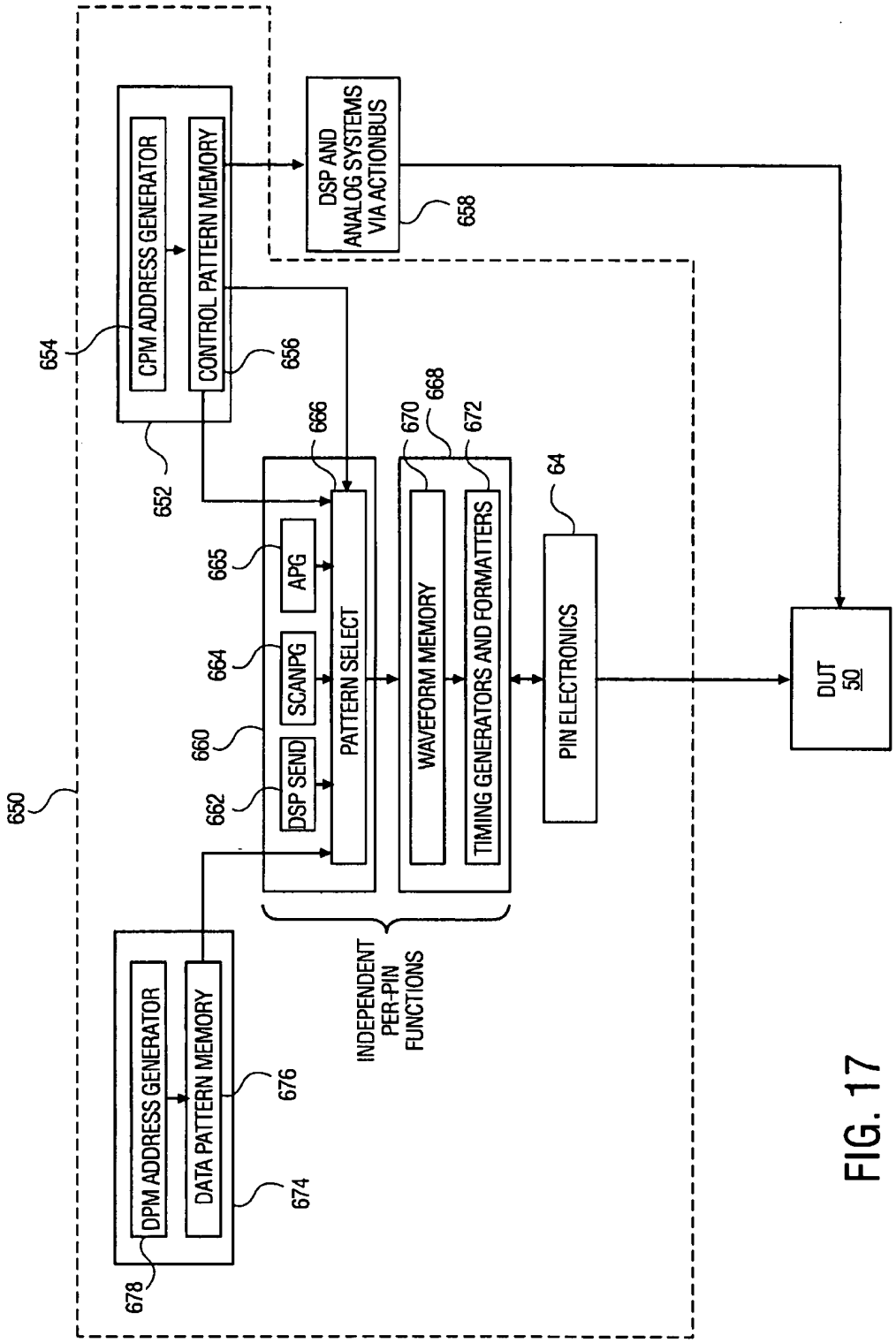
650
652
654
CPM ADDRESS GENERATOR
CONTROL PATTERN MEMORY
656
658
DSP AND ANALOG SYSTEMS VIA ACTIONBUS
660
662
664
665
666
668
670
672
64
DSP SEND
SCANPG
APG
PATTERN SELECT
WAVEFORM MEMORY
TIMING GENERATORS AND FORMATTERS
PIN ELECTRONICS
DUT 50
INDEPENDENT PER-PIN FUNCTIONS
676
674
678
DPM ADDRESS GENERATOR
DATA PATTERN MEMORY

FIG. 17

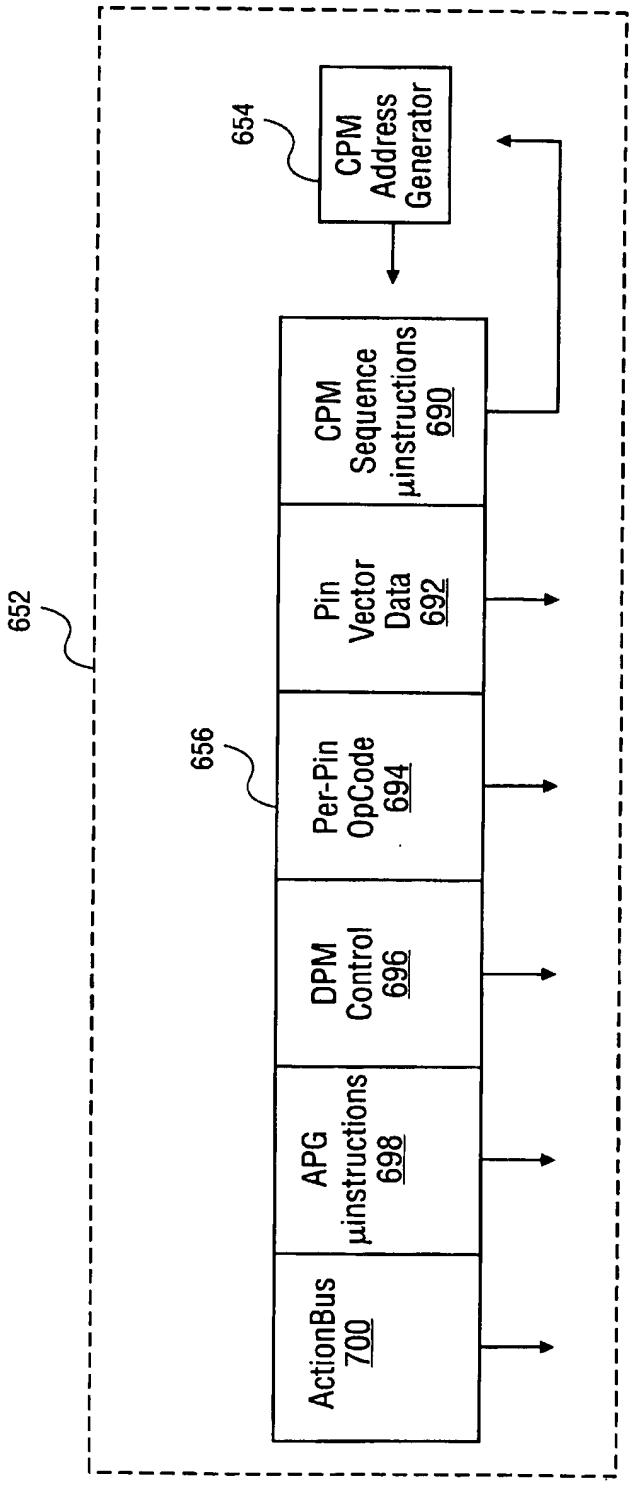
652
654
CPM Address Generator
CPM Sequence µinstructions 690
Pin Vector Data 692
656
Per-Pin OpCode 694
DPM Control 696
APG µinstructions 698
ActionBus 700

FIG. 18

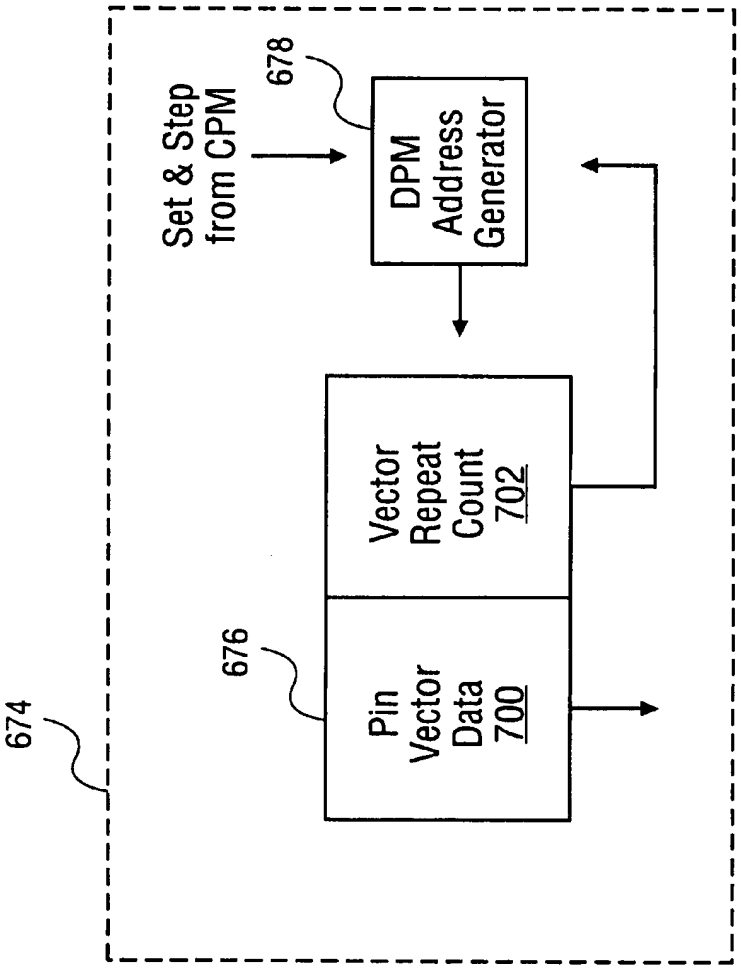
674
676
678
Set & Step from CPM
DPM Address Generator
Vector Repeat Count 702
Pin Vector Data 700

FIG. 19

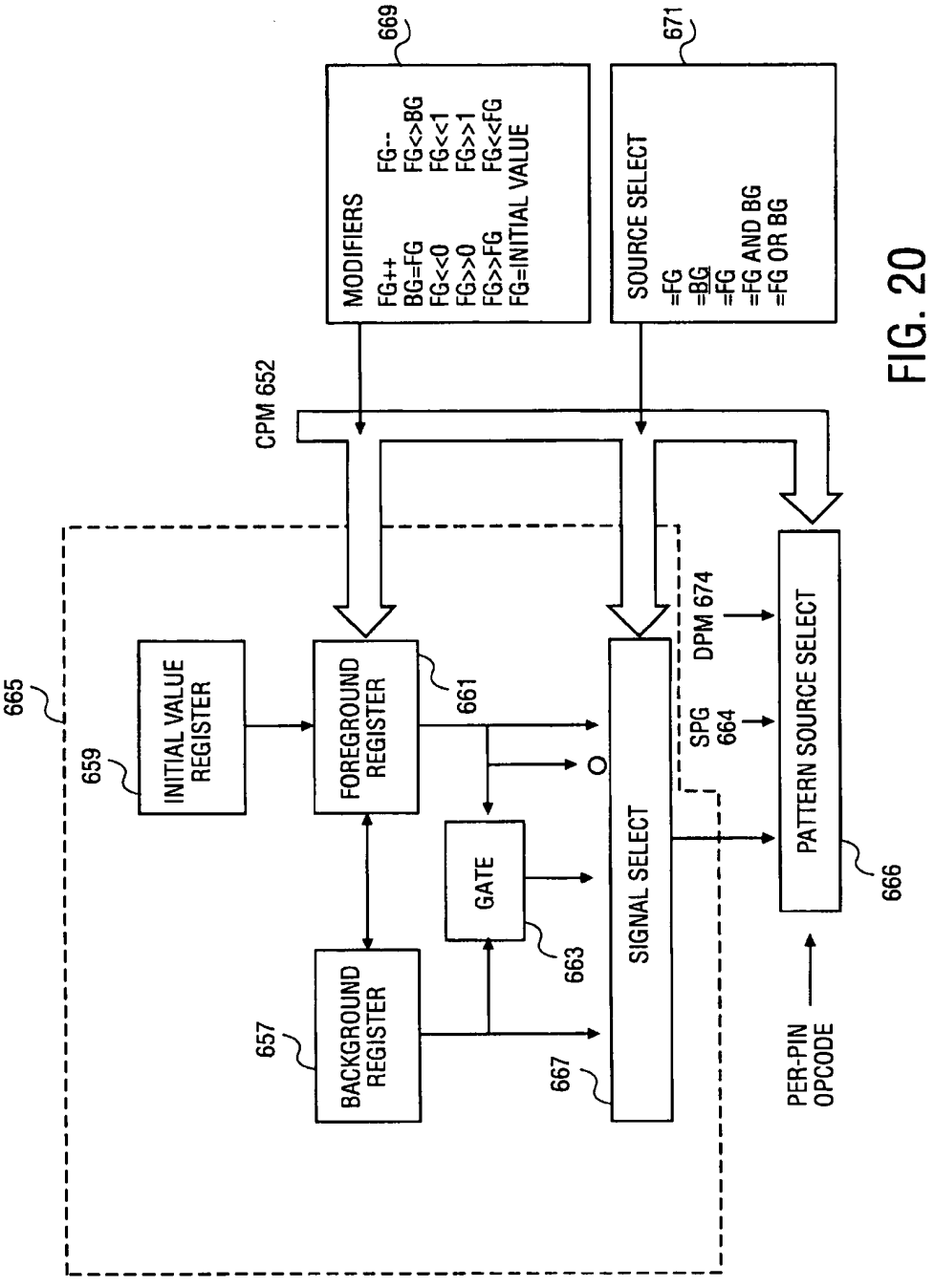
669
MODIFIERS
FG++
BG=FG
FG<<0
FG>>0
FG>>FG
FG=INITIAL VALUE
FG--
FG<>BG
FG<<1
FG>>1
FG<<FG
671
SOURCE SELECT
=FG
=BG
=FG
=FG AND BG
=FG OR BG
CPM 652
665
659
INITIAL VALUE REGISTER
FOREGROUND REGISTER
661
BACKGROUND REGISTER
657
GATE
663
SIGNAL SELECT
667
DPM 674
SPG 664
PATTERN SOURCE SELECT
666
PER-PIN OPCODE

FIG. 20

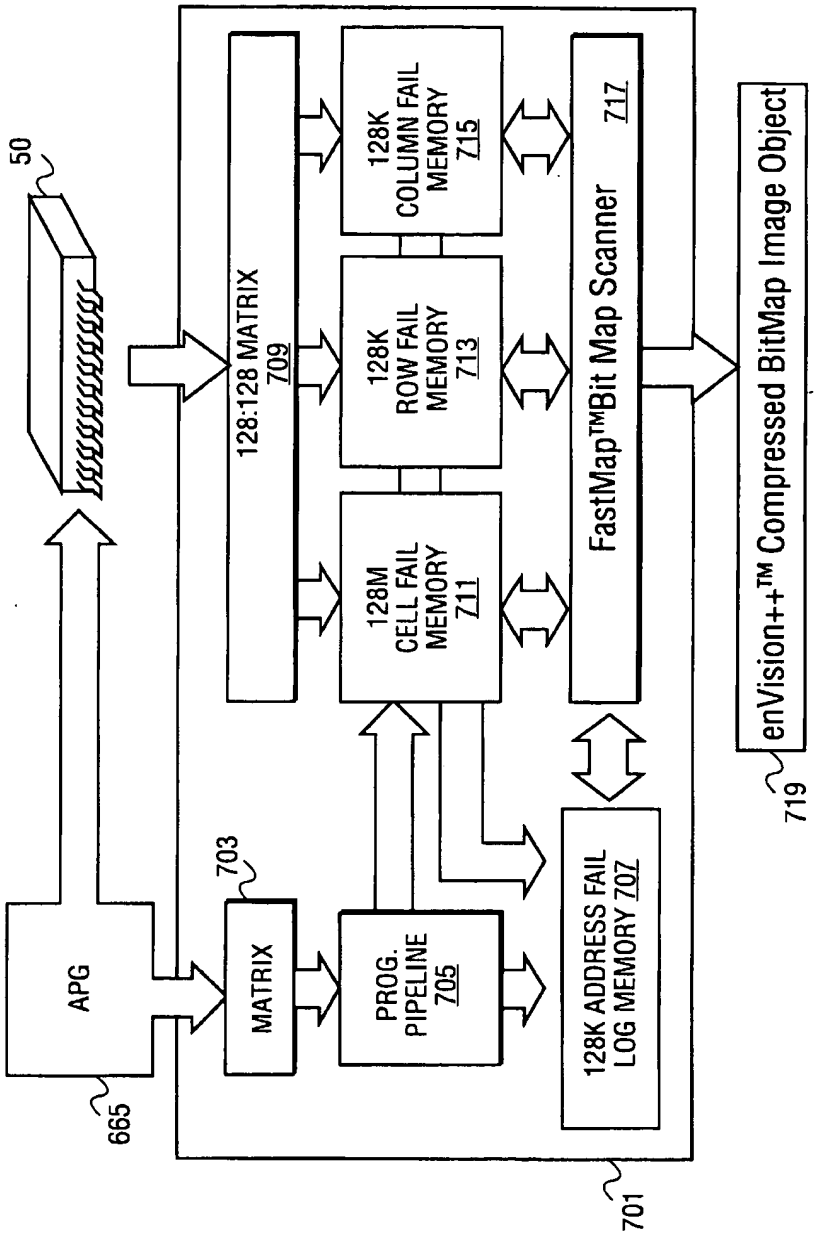
50
128:128 MATRIX 709
128K COLUMN FAIL MEMORY 715
128K ROW FAIL MEMORY 713
128M CELL FAIL MEMORY 711
FastMap™Bit Map Scanner 717
enVision++™ Compressed BitMap Image Object
719
APG
665
703
MATRIX
PROG. PIPELINE 705
128K ADDRESS FAIL LOG MEMORY 707
701

FIG. 21

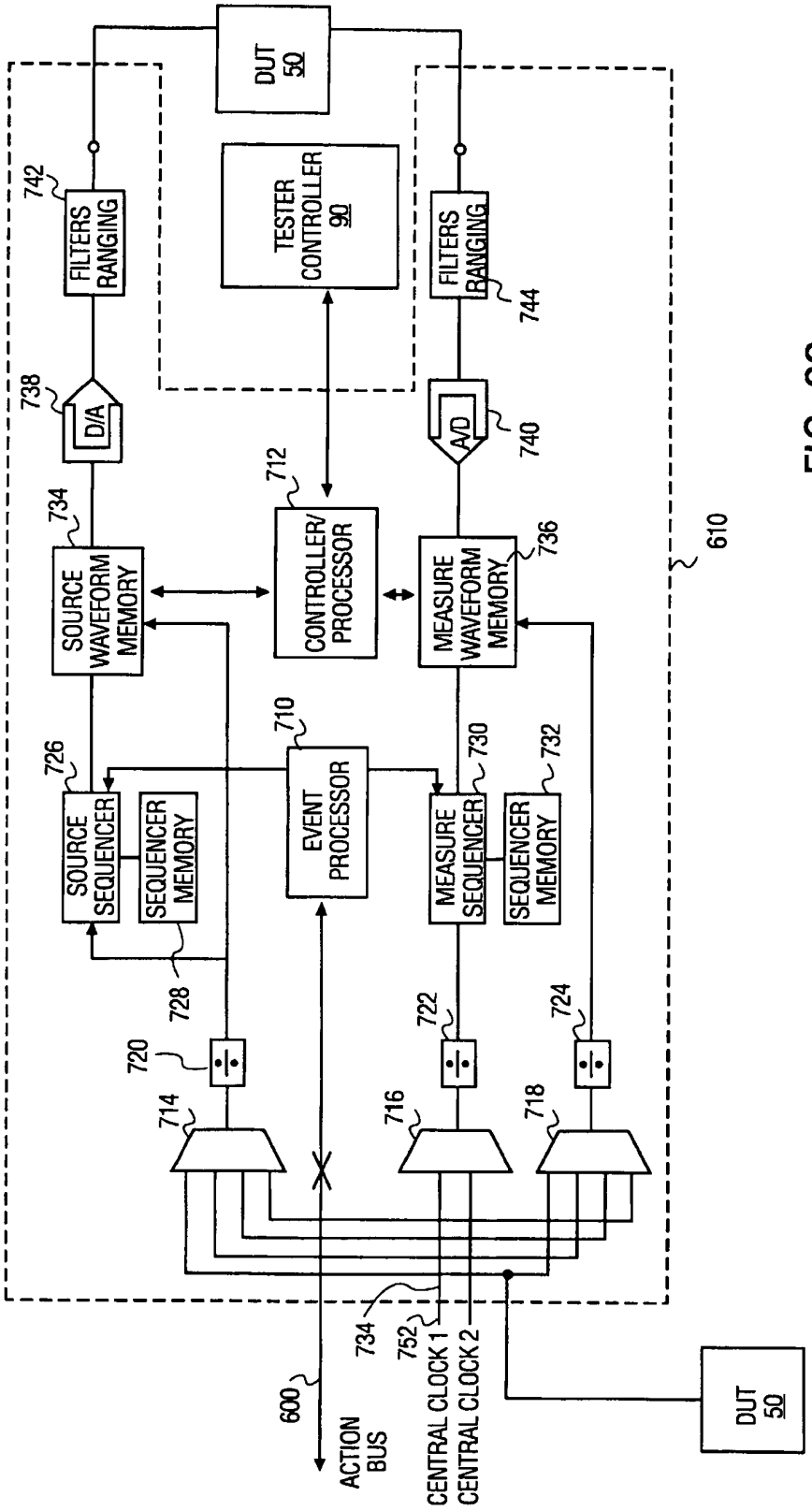
DUT 50
TESTER CONTROLLER 90
FILTERS RANGING
742
FILTERS RANGING
744
D/A
738
A/D
740
CONTROLLER/ PROCESSOR
712
SOURCE WAVEFORM MEMORY
734
MEASURE WAVEFORM MEMORY
736
610
EVENT PROCESSOR
710
SOURCE SEQUENCER
726
SEQUENCER MEMORY
MEASURE SEQUENCER
730
SEQUENCER MEMORY
732
728
720
722
724
714
716
718
600
ACTION BUS
734
752
CENTRAL CLOCK 1
CENTRAL CLOCK 2
DUT 50

FIG. 22

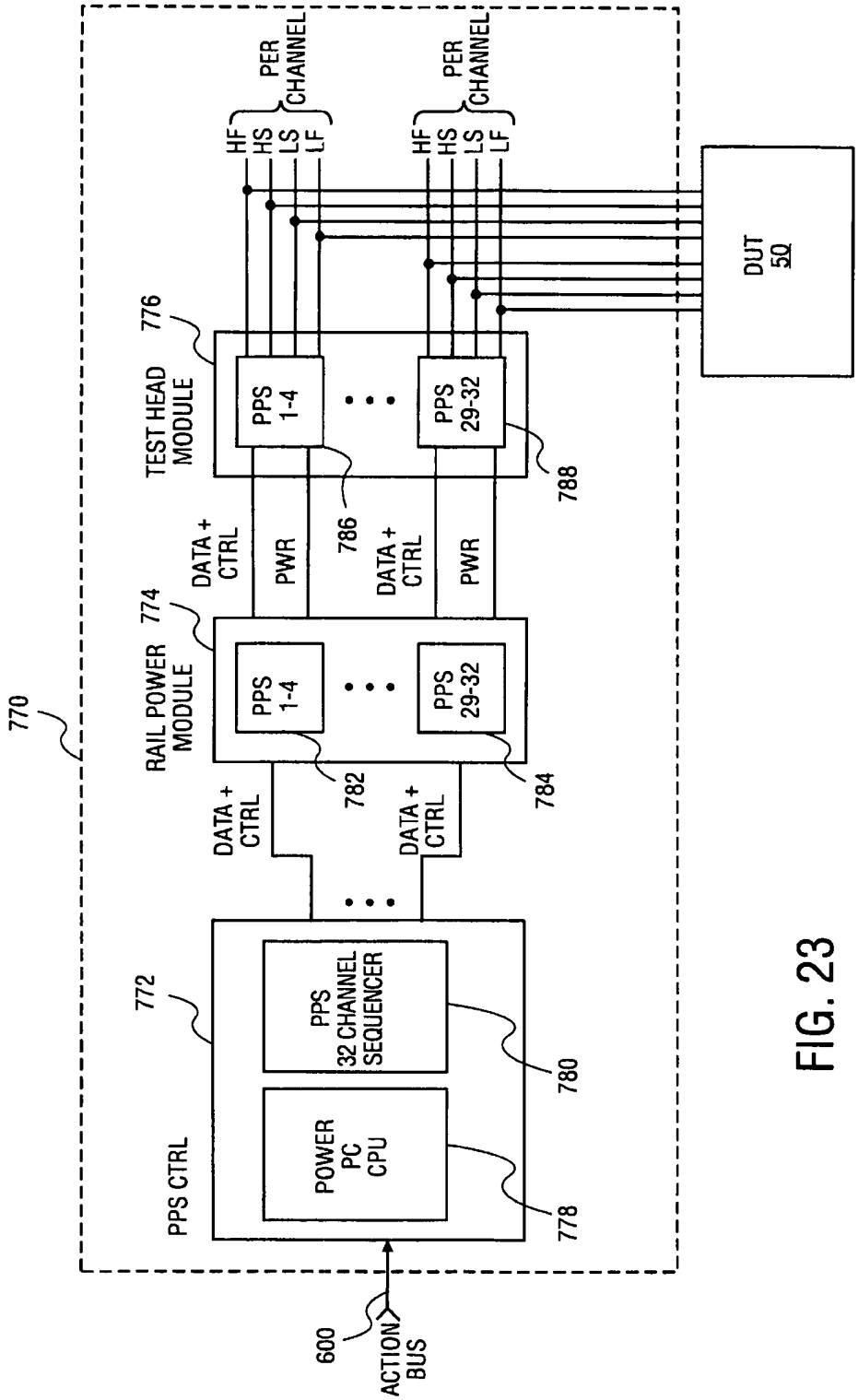
770
772
PPS CTRL
POWER PC CPU
778
PPS 32 CHANNEL SEQUENCER
780
600
ACTION BUS
774
RAIL POWER MODULE
PPS 1-4
PPS 29-32
782
784
DATA + CTRL
PWR
776
TEST HEAD MODULE
786
788
HF
HS
LS
LF
PER CHANNEL
DUT 50

FIG. 23

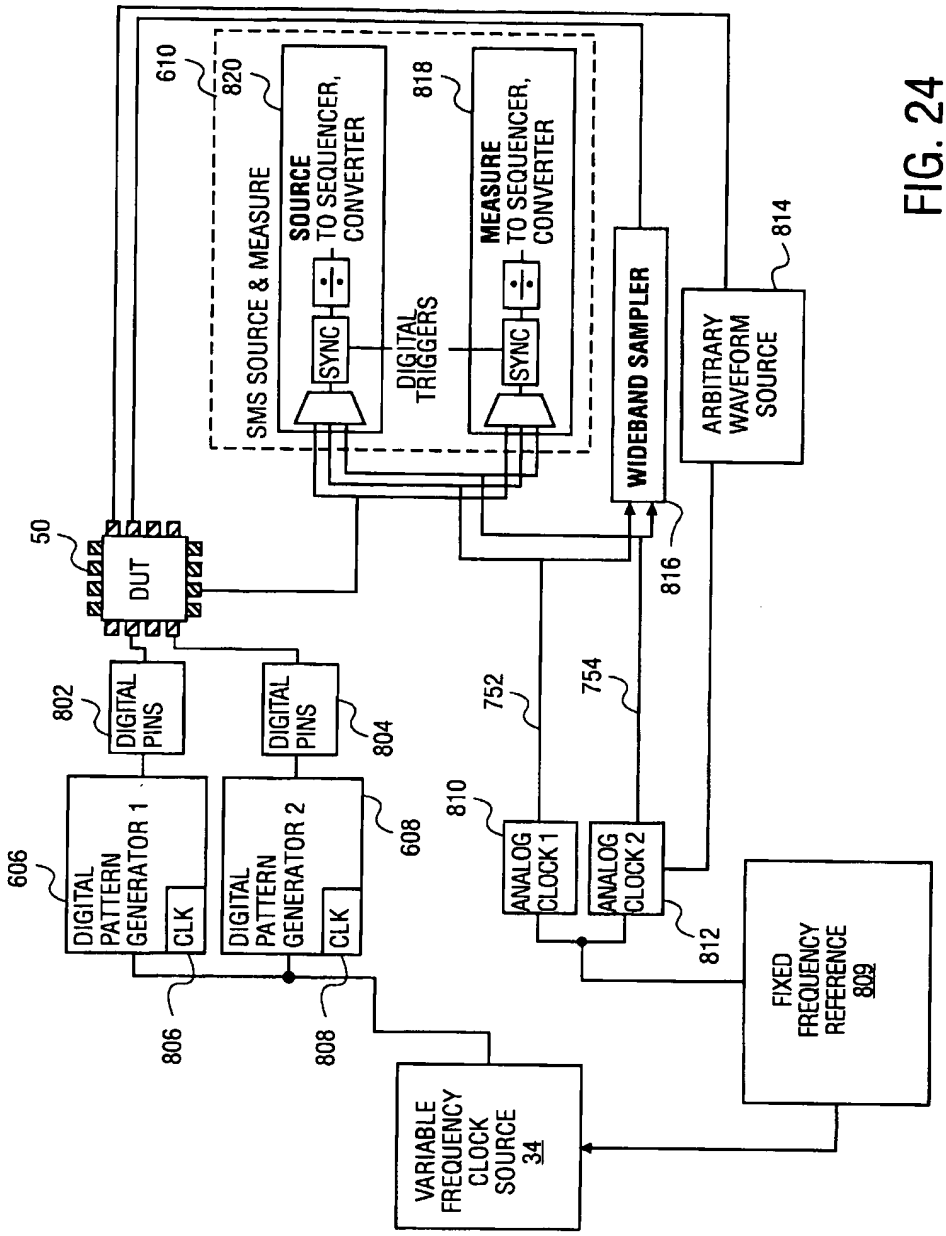
610
820
818
SMS SOURCE & MEASURE
SOURCE
TO SEQUENCER, CONVERTER
MEASURE
TO SEQUENCER, CONVERTER
SYNC
SYNC
DIGITAL TRIGGERS
WIDEBAND SAMPLER
ARBITRARY WAVEFORM SOURCE
814
50
DUT
816
802
DIGITAL PINS
804
DIGITAL PINS
752
754
606
DIGITAL PATTERN GENERATOR 1
CLK
608
DIGITAL PATTERN GENERATOR 2
CLK
810
ANALOG CLOCK 1
ANALOG CLOCK 2
812
FIXED FREQUENCY REFERENCE 809
806
808
VARIABLE FREQUENCY CLOCK SOURCE 34

FIG. 24

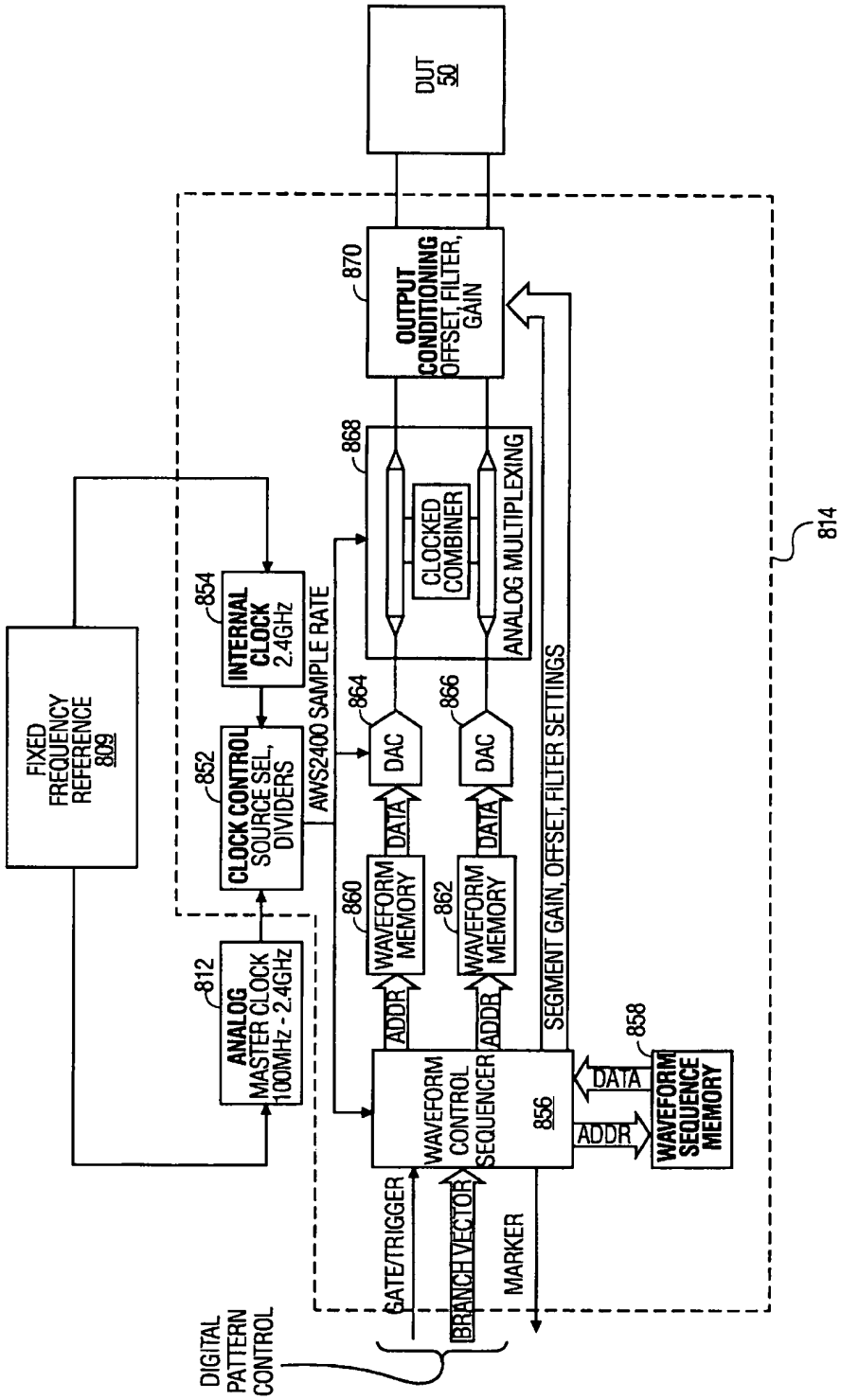
DUT
50
814
870
OUTPUT
CONDITIONING
OFFSET, FILTER,
GAIN
868
CLOCKED
COMBINER
ANALOG MULTIPLEXING
854
INTERNAL
CLOCK
2.4GHz
FIXED
FREQUENCY
REFERENCE
809
852
CLOCK CONTROL
SOURCE SEL,
DIVIDERS
AWS2400 SAMPLE RATE
864
DAC
866
DAC
DATA
DATA
860
WAVEFORM
MEMORY
862
WAVEFORM
MEMORY
812
ANALOG
MASTER CLOCK
100MHz - 2.4GHz
ADDR
ADDR
SEGMENT GAIN, OFFSET, FILTER SETTINGS
858
WAVEFORM
CONTROL
SEQUENCER
856
DATA
ADDR
WAVEFORM
SEQUENCE
MEMORY
GATE/TRIGGER
BRANCH VECTOR
MARKER
DIGITAL
PATTERN
CONTROL

FIG. 25

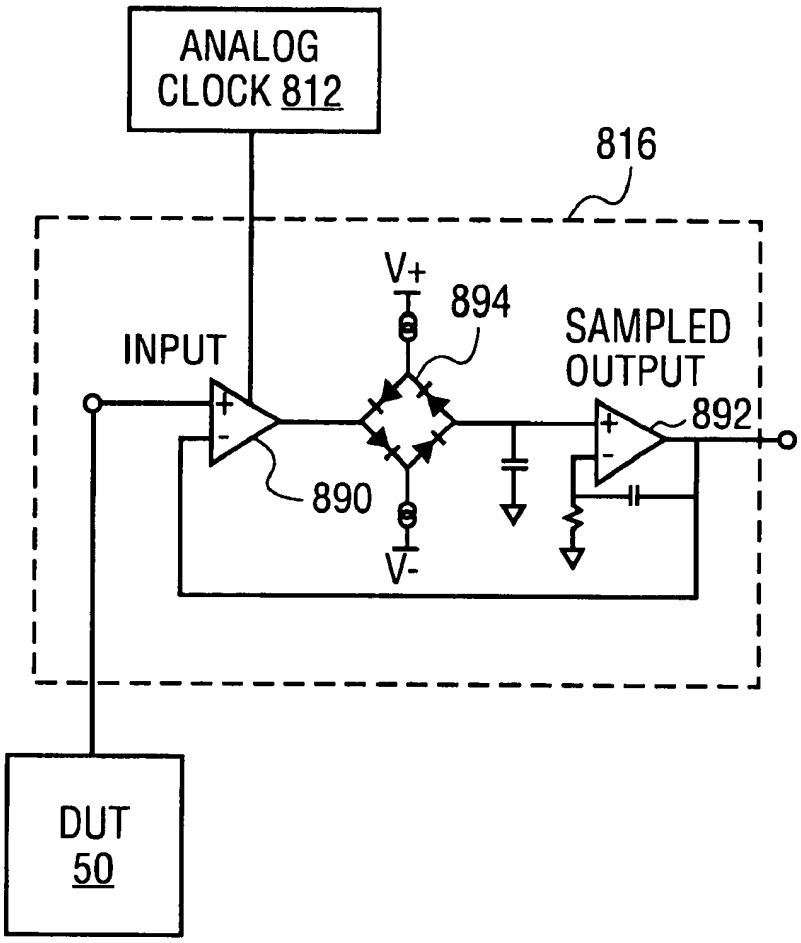
ANALOG
CLOCK 812
816
V+
894
INPUT
SAMPLED
OUTPUT
892
890
V-
DUT
50

FIG. 26

SINGLE PLATFORM ELECTRONIC TESTER

FIELD OF THE INVENTION

The present invention pertains to the field of electronic test equipment for testing integrated circuits. More particularly, the present invention relates to a single platform electronic tester that includes both digital, analog, and memory test circuitry for testing integrated circuits having digital circuitry, memory circuitry, and analog circuitry.

BACKGROUND OF THE INVENTION

Automatic electronic test equipment has been used to test various types of integrated circuits ("ICs") and discrete semiconductor components.

The different types of integrated circuits have included digital ICs, linear ICs, and mixed signal ICs. Examples of digital ICs include high-speed very large scale integrated ("VLSI") digital ICs, including microprocessors and microcontrollers. Linear ICs are also called analog ICs. Linear ICs are used, for example, to amplify, filter, or shape information such as sound, images, temperature, pressure, speed, acceleration, position, or rotation. Examples of linear ICs include amplifiers, voltage regulators, voltage detectors, operational amplifiers, clock circuits, and phase locked loops. Mixed signal ICs handle both digital and analog signals. One example of a mixed signal IC is a D to A converter that converts digital signals to analog signals. Another type of mixed signal IC is an A to D converter that converts analog signals to digital signals.

Different prior art automatic test equipment has been used to test different categories of ICs. Digital automatic test systems have been used to test digital ICs. Linear/mixed signal automatic test systems have been used to test linear and mixed signal ICs.

One example of a prior art digital test system is the Micromaster™ sold by LTX Corporation of Westwood, Mass. The Micromaster is designed for testing high performance CISC (complex instruction set computing) and RISC (reduced instruction set computing) microprocessors and the digital ICs that make up the chip sets that are used with the microprocessors.

One example of a prior art linear/mixed signal test system is the Synchro™ test system sold by LTX Corporation of Westwood, Mass. The Synchro automatic test system is designed for high throughput testing of linear ICs and for testing of mixed signal ICs that require lower digital pattern rates and moderate digital pin counts. The Synchro tester includes independent microprocessors that concurrently control each test instrument applied to the device under test (i.e., the IC under test). This design permits the generation of test signals and measurements on many device pins at the same time in order to speed up test times on high complexity ICs.

Trends in technology have resulted in more circuits, transistors, and other devices being placed on integrated circuits. In other words, the level of chip integration has risen. Because of this, a new category of integrated circuit has arisen, called the system-on-a-chip ICs. System-on-a-chip ICs are also referred to as multifunction ICs or multifunction devices. The system-on-a-chip ICs integrate fundamentally different IC subsystems on the same piece of silicon. These IC subsystems include VLSI logic cores, embedded memory, and mixed signal interfaces. Thus, system-on-chip ICs can incorporate digital circuitry, analog circuitry, and memory circuitry on a single chip. These subsystems were once available only on a circuit board populated with discrete devices, but now are placed on a single IC. One example of a system-on-a-chip is the Riva™ 128 graphics controller sold by nVidia, Inc., Inc. of Santa Clara, Calif. The Riva 128 is a single chip implementation of a graphics accelerator that digitally manipulates video images and then transmits them in analog form to either a computer or a television monitor.

One disadvantage of the prior art automatic electronic testers is that no single tester has the performance required to test a broad range of digital ICs, analog/mixed signal ICs, and memory ICs. To test a broad range of such types of ICs, a company would have to purchase at least two types of testers and train personnel to use at least two types of testers.

Prior art digital testers and prior art linear/mixed signal testers typically have some complementary technology, however. The prior art linear/mixed signal testers typically have some limited digital testing capability. The prior art digital testers typically have some limited analog capability. Nevertheless, complementary capabilities of both types of testers is extremely limited. Furthermore, the two types of testers are typically incompatible. This can result in higher cost of operation because test equipment is underutilized when the device that the tester can exclusively test is not being produced.

As a result, the primary disadvantage of prior art electronic test equipment is that a single platform tester cannot fully test the full spectrum of ICs, including some of the more complex ICs that have a high level of integration, such as some newer system-on-a-chip ICs. In other words, one would have to use both a digital automatic electronic tester and a linear/mixed signal automatic electronic tester to fully test certain complex multifunction ICs. Using two testers is typically relatively expensive, cumbersome, and time consuming as opposed to using a single tester. Not only is there the added expense of two machines rather than one, but typically corporations have employees who are trained on one type of tester (digital or linear/mixed signal) but not the other, and vice versa. Furthermore, some tests might be extremely difficult, if not impossible, to perform on two separate testers sequentially if there is high level of integration between analog circuitry and high speed digital circuitry on a single chip. Moreover, in certain instances, prior art testers are not capable of testing the new types of functions performed by single multifunction ICs, especially those functions that occur at increasingly high speeds.

SUMMARY AND OBJECT OF THE INVENTION

An object of the present invention is to provide a single electronic tester for testing digital integrated circuits, analog integrated circuits, mixed signal integrated circuits, and system-on-a-chip integrated circuits.

Another object of the invention is to provide an electronic tester that has a modular implementation of hardware and software of the tester.

An electronic tester is described that has digital, analog, and memory test circuitry on a single platform. A test head is coupled to a device under test. The device under test can be a system-on-a-chip integrated circuit, a mixed signal

integrated circuit, a digital integrated circuit, or an analog integrated circuit. Digital test circuitry applies digital test signals to the device under test coupled to the test head and receives digital outputs from the device under test in response to the digital test signals. Analog test circuitry applies analog test signals to the device under test coupled to the test head and receives analog outputs from the device under test in response to the analog test signals. Memory test circuitry applies memory test patterns to the device under test coupled to the test head and receives outputs from the device under test in response to the memory test patterns. A tester computer supervises the application of digital, analog, and memory test signals from the digital, analog, and memory test circuitry to the device under test such that signals applied to the device under test can be solely digital test signals, solely analog test signals, solely memory test patterns, or mixed digital test signals, analog test signals, and memory test patterns. The test head, the digital circuitry, the analog circuitry, the memory test circuitry, and the computer are operable as a single platform.

Other objects, features, and advantages of the present invention will be apparent from the accompanying drawings and from the detailed description that follows below.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention is illustrated by way of example and not limitation in the figures of the accompanying drawings, in which like references indicate similar elements, and in which:

FIG. **1** is block diagram of a single platform electronic tester for testing digital ICs, analog ICs, mixed signal ICs, and system-on-a-chip ICs.

FIG. **2** illustrates an electronic tester test head that holds both digital test boards and analog test boards.

FIG. **3** is a block diagram of the electronic tester that shows various data and control buses.

FIG. **4** is a block diagram of the electronic tester that shows the configuration of the network interface computer with respect to the tester controller, the test process accelerator, and the digital and analog boards of the test head.

FIG. **5** illustrates an action packet of the electronic tester.

FIG. **6** shows tools and data objects of the network interface computer of the electronic tester.

FIG. **7** shows the graphical user interface of the launcher of the electronic tester.

FIG. **8** shows the graphical user interface of the operator tool of the electronic tester.

FIG. **9** shows the graphical user interface for the icon palette of test methods for the electronic tester.

FIG. **10** shows the graphical user interface of the flow tool of the electronic tester.

FIG. **11** shows the graphical user interface of the test tool for the electronic tester.

FIG. **12** shows the graphical user interface of the find feature of the test tool for the electronic tester.

FIG. **13** shows the graphical user interface for the editor and debugger of the electronic tester.

FIG. **14** shows the graphical user interface for selecting an analog software routine from the microflow tool of the electronic tester.

FIG. **15** shows the graphical user interface for finding an analog software routine from the method tool of the electronic tester.

FIG. **16** illustrates the action bus architecture of the electronic tester.

FIG. **17** is a block diagram of digital test circuitry of the electronic tester.

FIG. **18** is a block diagram of the control pattern memory processing unit of the electronic tester.

FIG. **19** is a block diagram of the data pattern memory processing unit of the electronic tester.

FIG. **20** is a block diagram of the algorithmic pattern generator of the electronic tester.

FIG. **21** is a block diagram of the fail log memory of the electronic tester.

FIG. **22** is a block diagram of the sequenced measure system of the electronic tester.

FIG. **23** is a block diagram of the pulsed power source of the electronic tester.

FIG. **24** is a block diagram of the clocking architecture of the electronic tester.

FIG. **25** is a block diagram of the arbitrary waveform source of the electronic tester.

FIG. **26** is a diagram of the wideband sampler of the electronic tester.

DETAILED DESCRIPTION

A single platform electronic tester is described that can test digital integrated circuits, analog integrated circuits, mixed signal integrated circuits, and system-on-a-chip integrated circuits. Various aspects of the single platform electronic tester are described in more detail below. A computer of the tester causes a tester controller to send action packets to analog test circuitry to execute analog tests of a device under test ("DUT"). The computer also causes the digital test circuitry to execute digital tests of the DUT.

The electronic tester of one embodiment includes a system of distributed processing, synchronization, and highly interchangeable components. An intended advantage is to provide a highly flexible tester that can be relatively quickly and easily reconfigured to test digital ICs, analog ICs, mixed signal ICs, or system-on-a-chip ICs. An intended advantage of this approach is to scale tester cost and size more exactly to the requirements of the particular integrated circuits being tested.

A computer-generated graphical user interface of the electronic tester allows a user to launch an operating system of the electronic tester that can execute digital and analog test programs. As described in more detail below, a graphical user interface of the electronic tester allows the memory components, digital components, and analog components of a test program to automatically execute one followed by the other. Any number of memory components, digital components, and analog components can follow each other. Furthermore, the digital, analog, and memory components of a test program can execute concurrently.

The electronic tester also includes a computer that can display a graphical user interface that allows a user to see and arrange the flow of test program execution that contains digital, analog, and memory test components. The electronic tester also includes a graphical user interface that allows the user to display source code of the analog, memory, and digital test program components and a graphical user interface that allows debugging of the memory, digital and analog test program components.

In the electronic tester, digital test procedures can be called from an analog test program and analog test procedures can be called from a digital test program.

The electronic tester also includes special timing circuitry to help to ensure proper synchronization. A component of the electronic tester, acting as a master, sends a timing marker over a marker bus. A modular test circuit retrieves the timing marker from the marker bus. The modular test circuit starts a test on a DUT upon receipt of the timing marker. The test is controlled by a test sequence predefined for the modular test circuit prior to retrieval of the timing marker by the modular test circuit.

Clocking circuitry of the electronic tester is also described in more detail below. Each digital test circuit has a high speed clock generator. That high speed clock generator generates a clock having a frequency that is adjustable in multiples of an input frequency. A variable frequency clock provides an input frequency for the clocks of the digital test circuitry. The variable clock generator has a continuously adjustable clock frequency that determines the input or reference frequency for each of high speed clock generators coupled to the digital test circuits. Analog circuits are coupled to high speed analog clocks. Both the digital variable reference clock and the analog high speed clocks are referenced to a single, fixed frequency reference in order to provide frequency coherence among the various elements of the test system. The fixed frequency reference is a low speed clock.

A discussion of the hardware and software of the electronic tester is set forth below in connection with FIGS. **1–6**. A discussion of the graphical user interfaces of the electronic tester is set forth in connection with FIGS. **7–15**. The action bus of the electronic tester is described in connection with FIG. **16**. Digital and memory test circuitry is described in connection with FIGS. **17–21**. Analog test circuitry of the electronic tester is described in connection with FIGS. **22–23**. Clocking circuitry and associated circuitry of the electronic tester is discussed in connection with FIGS. **24–26**.

FIG. **1** is a block diagram of electronic tester **10** with digital and analog test circuitry for testing device under test **50**. Electronic tester **10** is a single platform tester. Electronic tester **10** includes test head **16** that includes connector pins for receiving device under test **50**. Device under test **50** can be a system-on-a-chip integrated circuit, a mixed signal integrated circuit, a digital integrated circuit, and IC memory, or an analog integrated circuit. For an alternative embodiment of the invention, electronic tester **10** includes a second test head.

The main body **12** of electronic tester **10** includes cooling equipment **38**, digital test circuitry **20**, power supply **24**, analog test circuitry **22**, bus adapters **26**, processor cards **28**, multimeter **30**, time measurement unit **32**, frequency synthesizer **34**, and power supply **36**. Refrigeration unit **40** is coupled to cooling equipment **38** via refrigeration line **42**.

Network interface computer **14** controls the overall operation of electronic tester **10** and is coupled to main body **12**. Network interface computer **14** includes a central processing unit ("CPU") **44**, cathode ray tube ("CRT") **46**, keyboard **48**, and mouse **49**. For one embodiment of the present invention, network interface computer **14** is a SPARC™ workstation sold by Sun Microsystems of Mountain View, Calif.

Digital test circuitry **20** is the test circuitry used to generate test vectors sent to device under test **50**. Digital test circuitry **20** includes a card cage that for one embodiment holds 16 printed circuit boards. Each printed circuit board has 16 digital pattern generators. Digital circuitry **20** has four racks of card cages, for a total of 64 printed circuit boards, wherein each printed circuit board has 16 digital pattern generators. The control pattern memory processing unit **652** uses a flexible set of microinstructions to generate complex pattern sequences that require looping, conditional branching, and nested subroutines. The control pattern memory processing unit **652** also provides microinstruction control over per pin pattern source selection, data pattern memory sequencing, and algorithmic pattern generator algorithms. The digital pattern memory processing unit **674** provides long sequential vector patterns with vector repeat capabilities, which allows engineers to simulate digitally intensive devices. Each digital pattern generator is a customized integrated processor that executes assembly codes step by step upon receipt of clock input. The digital pattern generators are microcoded. Thus, each digital pattern generator operates as a sequencer.

Each digital pattern generator of digital test circuitry **20** includes a control pattern memory processing unit **652** and a data pattern memory processing unit **674**.

The digital pattern generators of digital circuitry **20** can drive 1,024 pins of DUT **50** in parallel. For one embodiment, the digital pattern generators of digital circuitry **20** operate at speeds up to 500 megahertz.

For one embodiment, digital test circuitry **20** also includes algorithmic pattern generator ("APG") **665** for producing patterns for testing embedded memory arrays of DUT **50**. Digital test circuitry **20** further includes fail log memory **710** for capturing accumulated failures, which is used for testing memories.

Analog test circuitry **22** includes circuitry for sending and receiving analog signals with respect to DUT **50**. Analog test circuitry **22** includes sequenced measure system™ ("SMS") **610**. Sequenced measure system **610** features analog performance from direct current ("DC") to 100 megahertz and local digital signal processing ("DSP") that eliminates data transfers through electronic testor **10**. For one embodiment, the sequenced measure system **610** contains analog circuitry optimized for analog waveform operations up to 100 megahertz. For an alternative embodiment, sequenced measure system **610** is optimized for lower frequency higher precision operations. For one embodiment, a portion of SMS circuitry **610** also resides within test head **16**.

For one embodiment, analog test circuitry **22** also includes pulsed power source ("PPS") **770**. PPS **770** is a multi-channel high power voltage/current source designed to test smart power blocks on system-on-a-chip ICs. For one embodiment, a portion of PPS circuitry **770** also resides within test head **16**.

For one embodiment, analog test circuitry **22** also includes vector RF (radio frequency) source and measure unit **23**. The vector RF unit **23** provides basic scalar source and measure, modulation, and vector network measurements such as S parameters with respect to DUT **50**. For one embodiment, a portion of vector RF unit circuitry **23** resides within test head **16**. Vector RF unit **23** is used for testing single-chip transceivers, IQ modulators and demodulators, power amplifiers, VCOs, mixers, LNAs, synthesizers, and phase-lock loops ("PLLs"), for example.

Bus adapters **26** of electronic tester **10** are interfaces between various types of buses used within electronic tester **10**. Processor cards **28** include the microprocessors used within electronic tester **10** to perform various functions.

Multimeter **30** is used as a voltage tester to measure various signals, including signals coming to and from DUT **50**. For one embodiment of the invention, multimeter **30** is an HP multimeter sold by Hewlett Packard, Inc. of Palo Alto, Calif.

Time measurement unit **32** is a four channel precision time measurement system with a local processor. This system contains two special gate channel inputs in addition to the start and stop channels through which it can accept gating signals, timing strobes, and timing patterns from external sources. Start and stop events from DUT **50** can be synchronized with the third DUT output or with another timing source such as a digital pin. For one embodiment, the time measurement unit **32** is sold by Wavecrest Inc. of Edina, Minn.

Time measurement unit **32** also contains a programmable hold off counter (not shown) that allows time measurement unit **32** to measure time intervals within a sequence of events specified for the test engineer, including near simultaneous start/stop events. Testing can start and stop anywhere on a leading edge, a trailing edge, after a timing event, or after a series of events.

Frequency synthesizer **34** generates a variable speed clock for the digital test circuitry **20** of electronic tester **10**. For one embodiment of the present invention, frequency synthesizer **34** is a PTS 310D synthesizer sold by Programmed Test Sources of Littleton, Mass. The frequency of the frequency synthesizer **34** can be adjusted.

Power supplies **24** and **36** of electronic tester **10** supply power to various circuitry of electronic tester **10**.

Refrigeration unit **40** and cooling equipment **38** is used to circulate liquid to cool electronic circuitry of electronic tester **10**.

FIG. **2** illustrates test head **16** of electric tester **10**. Device under test **50** resides on a custom DUT board **70** that is installed on test head **16**. DUT card **70** is a custom designed printed circuit card that has circuit traces that electrically connect to metallic pogo pin contacts found in connector fields **66** and **68**.

Connector field **66** is made up of digital metallic connector pins that are coupled to respective digital pin electronic cards **64** that reside on the bottom of test head **16**. Connector field **68** is made up of metallic connector pins that are coupled to respective analog test boards **62** that reside in the front of test head **16**. Each of the pins in the analog connector field **68** is optimized for the type of analog signal being transmitted. For example, coaxial connectors are used for RF signals to facilitate high bandwidth, low loss, blind-mate connections.

For one embodiment of the invention, test head **16** includes 1,024 digital pogo pins within digital connector pin ring **66**. For one embodiment, 500 analog connections reside within analog connector field **68**.

System configuration module™ ("SCM") board **80** maps tester resources to DUT board **70** and allows for market specific customization of signal circuitry for testing families of devices. For one embodiment, test head **16** can hold **32** analog or mixed signal boards **62**. Analog boards **62** are also called mixed signal boards **62**. For one embodiment of the present invention, analog boards **62** are custom designed for the user to perform the desired analog or mixed signal test with respect to DUT **50**. SCM board **80** includes relays and capacitors for switching analog signals between analog board **62** and DUT **50**. For one embodiment of the present invention, SCM board **80** is custom designed by the user to achieve the desired analog or mixed signal test with respect to the DUT **50**. Outer analog connector field contains 500 analog connections and is coupled to SCM board **80**.

Test head **16** can hold 64 pin electronics cards **64**. Digital pin electronics cards **64** are configured in a circular pattern underneath DUT board **70**. Digital pin electronic cards **64** provide relatively high bandwidth source and measure. Digital pin electronic cards **64** have relatively fast and programmable rise and fall times. Clock pulse widths go down to 600 picoseconds for one embodiment. The pin electronics cards **64** include an interface that provides a two-nanosecond electrical distance between any one of the 1,024 digital channels and the DUT **50** socket. Pin electronics cards **64** have the ability to generate low voltage driver voltage swings of as little as 50 millivolts for one embodiment. Pin electronics cards **64** include high bandwidth comparators, with 1.0 gigahertz a typical terminated bandwidth for one embodiment. Pin electronics cards **64** include circuitry to limit overshoot caused by impedance mismatches.

For one embodiment, pin electronics cards **64** include a differential drive and compare circuitry. In the differential drive mode, one set of data is fed into two drivers. One of the drivers inverts the data resulting in an accurate differential signal. Because the drivers are on the same piece of silicon, the signals are affected equally by drift and interference so they stay matched. A differential comparator determines the difference between the inputs so it is able to ignore common mode signals. Circuitry subtracts the voltages without assigning a binary state and a dual threshold comparator can determine whether the signal passes the voltage thresholds.

For one embodiment of the invention, test head **16** also includes 8 slots for accommodating radio frequency ("RF") and power modules. Each of the eight module slots **82** on test head **16** contains shielded, high bandwidth connectors for RF, and high current connectors for power.

Test head **16** also includes liquid cooling manifolds **76**.

FIG. **3** shows the bus structure and overall architecture of electronic tester **10**. The embodiment shown in FIG. **3** includes a second optional test head **18** for testing a second DUT.

Network interface computer **14** is coupled to Sbus **102**. Bus adapter **104** couples Sbus **102** to VME bus **106**. Tester controller **90** is coupled to VME bus **106**.

Tester controller **90** includes pacemaker circuitry **92** for establishing timing and providing an independent clock reference.

Bus adapter **108** couples VME bus **106** to Cbus/Ebus **124**. Analog resources **96** are coupled to Cbus/Ebus **124**. Analog resources **96** are also coupled to test heads **16** and **18**. Analog resources **96** include circuitry for doing analog source and measure tests with respect to test heads **16** and **18**.

Test process accelerator **110** is coupled to both VME bus **106** and VSB bus **112**. Bus adapter **126** is coupled to VSB bus **112** and GLINK bus **122**. GLINK bus **122** is in turn coupled to test head interfaces **98** and **100**. Test head interface **98** is coupled to test head **16** and test head interface **100** is coupled test head **18**.

Bus adapter **114** is coupled to both VSB bus **112** and Trillium bus **116**. Bus adapter **118** is coupled to Trillium bus **116** and digital backplane bus **120**.

Digital backplane bus **120** is coupled to digital resources **94**. Digital resources **94** are coupled to test heads **16** and **18**. Digital resources **94** are used for high speed testing with respect to digital data.

FIG. **4** is a view of the architecture of electronic tester **10** with respect to network interface computer **14**, tester controller **90**, test process accelerator **110**, analog boards **62**, and digital boards **64**.

Network interface computer **14** oversees digital tests, and analog tests, and memory tests with respect to device under

test **50** located in test head **16**. For analog tests, network interface computer **14** sends a signal to tester controller **90** via bus adapter **104** requesting that tester controller **90** initiate an analog test with respect to DUT **50**. Pacemaker **92** is part of tester controller **90**. Pacemaker **92** establishes timing for the analog test. Pacemaker **92** provides an independent clock reference that analog boards **62** can obtain synchronization with respect to.

Cadence™ is the operating system for tester controller **90** for controlling analog tests with respect to DUT **50**. Cadence is also the name for the computer language for writing test programs for analog tests of DUT **50**.

To perform an analog test, tester controller sends an action packet **140** to bus adapter **108**, which in turn sends the action packet **140** to analog boards **62**. Analog boards **62** are coupled to test head **16** and in turn coupled to device under test **50**. Analog boards **62** contain circuitry for performing analog source and measure tests with respect to device under test **50**.

Action packet **140** is shown in more detail in FIG. **5**. Action packet **140** includes an identification number area **144** that identifies the test circuitry that is to perform a test and what function or action is to be taken by that test circuitry with respect to DUT **50**. For example, the sequenced measure system **610** would look at the identification number area **144** of action packet **140** to see if SMS **610** is to perform a test and to see what action is to be taken. Action packet **140** also includes a pin number area **146** for identifying the pin of DUT **50** that is to be tested. Action packet **140** includes an area **148** for the identification of the voltage that is to be applied to a pin (identified in area **146** of the action packet) of device under test **50**.

For an embodiment of the invention, action packet **150** also includes area **150** for providing additional information with respect to the analog test with respect to device under test **50**. For example, for a forcing voltage test, the additional information **150** would include the current range and the current clamp value.

Tester controller **90** of FIG. **4** is microprocessor controlled. For one embodiment, tester controller **90** includes a 68030 microprocessor sold by Motorola Corporation of Schaumburg, Ill. For one embodiment, the microprocessor of tester controller **90** executes the Cadence programming language. The Cadence programming language is available from LTX Corporation of Westwood, Mass. Cadence is a programming language that is similar to Pascal, but that is tailored for electronic test applications.

The action packets **140** sent by test controller **90** are destined for analog boards **62** shown in FIG. **4**. Analog boards **62** are also called test modules **62**. For one embodiment, at least one of the analog boards **62** contains either a 68000 series microprocessor sold by Motorola Corporation of Schaumburg, Ill. or a Power PC™ microprocessor sold by Motorola Corporation of Schaumburg, Ill.

Digital testing and memory testing of DUT **50** can occur concurrently with respect to analog testing of DUT **50**. Digital testing, analog testing, and memory testing of DUT **50** can also occur in a serial manner.

Network interface computer **14** also oversees digital testing and memory testing with respect to device under test **50** located in test head **16**. Network interface computer **14** sends a signal over bus adapter **104** to test processor accelerator **110**. Test process accelerator **110** in turn sends a signal over bus adapter **114** and bus adapter **118** to digital boards **64**. Digital boards **64** are also called digital pin electronics cards **64**. Digital boards **64** in turn apply digital test signals and memory test patterns to device under test **50** in test head **16** and monitor the response of DUT **50** to those digital test signals and memory test patterns. For one embodiment of the present invention, test processor accelerator **110** includes a 68040 microprocessor sold by Motorola Corporation of Schaumburg, Ill.

For one embodiment, network interface computer **14** is a SPARC workstation sold by Sun Microsystems of Mountain View, Calif. The operating system for network interface computer **14** is UNIX.

An enVision++ executive system **130** is the operating environment for network interface computer **14**. The enVision++ executive system **130** runs on top of UNIX.

Network interface computer **14** also includes a tester controller interface **132** that runs on top of UNIX. Tester controller interface **132** is the interface to the Cadence operating system of tester controller **90**.

Editor and debugger compiler **136** also runs on the UNIX operating system on network interface computer **14**. Editor and debugger compiler **136** allows the user to edit, debug, and compile both Cadence analog test programs and digital and memory test programs that run in the enVision++ executive system **130**. The editor portion of editor and debugger compiler **136** allows one to add and delete lines of source code. The debugger portion of editor debugger and compiler **136** allows one to debug the digital and analog test programs, for example, by allowing one to insert break points. The compiler portion of editor debugger and compiler **136** is line oriented and compiles the test programs and procedures.

Tester interface **134** also runs on UNIX on network interface computer **14**.

Tester interface **134** is also called the enVision++ launcher. Tester interface **134** allows one to start or launch the test program enVision++ environment by clicking launch button **138** with a computer mouse **49**. Tester interface **134** is also called the enVision++ launcher **134** or just lanucher **134**.

FIG. **6** shows some of the software components of network interface computer **14**. The enVision++™ executive system **130** is launched by the enVision++ launcher **134**. The enVision++ executive system **130** is also called the enVision++ software system, the enVision++ operating environment **130**, or the test program environment **130**. The enVision++ executive system runs on top of UNIX and is a visual operating system using OSF/Motif. enVision ++ includes a device oriented graphical user interface ("GUI"). By using an X Windows system, the enVision++ operating system may be run from any X Windows terminal or workstation capable of running X Windows. The enVision++ executive system **130** controls the digital test circuitry, the analog test circuitry, and the memory test circuitry of electronic tester **10**.

enVision++ operating system **130** is an object oriented platform. enVision++ **130** is tester architecture independent. enVision++ **130** uses an application-oriented test program information base. enVision++ **130** has a reusable, modular test program structure. enVision++ **130** uses real time interaction with no batch compilation. enVision++ **130** uses graphical user interfaces for all functions. enVision++ **130** includes off line simulation features. enVision++ **130** also includes integrated characterization tools. enVision++ **130** includes hierarchical waveform and pattern objects. enVision++ **130** uses distributed expression processor capabilities. enVision++ **130** also uses standardized methodology. enVision++ **130** relies on an application oriented structure of test information.

Operator tool **160** is used by the user to specify and load a test program. A test program is loaded by selecting start button **162** with mouse **49**.

A test program developed in the enVision++ executive system **130** consists of a set of objects, such as objects **176** through **184**, that are stored in shared memory **174** on the network interface computer **14**. Objects **176** through **184** are interconnected at the object level. Each of objects **176** through **184** can be viewed by means of an associated tool that provides visual display and modification of the object. Objects can include, for example, test objects, flow objects, spec objects, pattern objects, and levels objects.

An enVision++ test program running within the enVision++ executive system **130** is a database of test objects, such as digital waveforms, analog waveforms, and pin maps. There are several different classes of test information objects. Each object contains information about some part of the test program. All test objects except patterns are saved on a disk of network interface computer **14** in a compact ASCII syntax.

The test engineer builds a test program as a series of test objects and procedures using a graphical user interface to navigate the library of options. The tester interface resolves the test program for the specific tester configuration. In particular, the tester interface resolves the test information contained within the test information objects and procedures into specific tester data and commands. This software architecture lets the test engineer create test programs that are tester independent, eliminating the need to port and maintain multiple versions of the same tester program for different tester types. Different test programs can use common test objects and procedures.

Test objects can be hierarchical and refer to external object files. For example, the test engineer can maintain the test specification object as a separate file so that it can be used by several programs. This allows the test engineer to partition test program information in order to support common test specifications, patterns, timing, and device packages. The data contained within an object is application specific information and would be the same for different testers.

Test objects interact with or refer to other test objects. For example, a spec sheet object can contain the test specifications used by several programs. Upgrading the object updates all test programs using that object. Each data object can be viewed by means of an associated tool that provides for visual display and modification of the object.

No matter how an object is generated, interactively or through an ASCII mechanism, once in shared memory **174** the object, such as objects **176** through **184**, is viewed and manipulated with the same tools. Once loaded, the ASCII source files no longer need to be kept on line. A test program, when loaded, exists in the shared memory of network interface computer **14**. When a test program is saved to disk, the test program is transferred into the ASCII syntax for the objects. A test program object contains a list of all the other objects that make up the test program. When this test program is selected for loading, all of the objects that it contains are loaded back into shared memory **174** in executable form once again. Several test program objects may be created for a given test program thereby allowing variations of the test program to be made for different applications (such as for wafer sort and final test). It is possible, once into the enVision++ shared memory **174** environment, to selectively load objects from other test programs.

Once a program is saved, the user has the option of saving only the objects that have changed and links to the test program that contain all the unchanged objects,

When a program is loaded, the information is resolved into specific attributes of the selected tester. Tester resource allocation and rules checking is performed at this time. Pattern, waveform, and timing information is resolved into the specified tester implementations. Programs can also be loaded, resolved, and simulated off line.

The enVision++ executive system **130** provides a total system integration of multisite testing (parallel testing) capability for up to 32 sites for one embodiment.

STIL objects can be read into the enVision++ executive system **130** through a STIL reader and then modified and saved as enVision++ test objects.

Each test in an enVision++ program selects a test method from a library of test methods and provides the test specific parameters and conditions. The library is a collection of generic procedures that cover a spectrum of very large scale test applications. A test method provides a standardized predefined test process (e.g., a leakage test) that is intended to be common for all test programs.

Test methods **187** are procedural functions that are written in the C++ language to perform a certain test or classes of tests on the device under test **50**. Test methods **187** are stored in a library located on network interface computer **14** for inclusion into a test program via the test tool **166**. The test methods **187** are complete and designed with necessary debug and characterization options.

The enVision++ executive system **130** allows the test engineer to write additions **189** to test methods **187**. The user additions are written in the C++ language. The test engineer is typically given the source code and can make variations to the source code. Test engineers can also write their own code and create their own objects, although for one embodiment new object types cannot be created by a test engineer. For an alternative embodiment, new object types can be created by a test engineer.

Cadence procedures (also referred to as Cadence test components) are analog test procedures with respect to DUT **50** that are written in the Cadence language and executed by tester controller **90** (shown in FIG. **4**). A Cadence module contains Cadence test procedures.

The enVision++ executive system **130** shown in FIG. **6** includes an expression processor. The expression processor of the enVision++ executive system **130** is software from the software library of the enVision++ executive system **130** that executes formulas or expressions. The expression processor allows expressions or formulas to be used in any place where a constant value would normally be used. This includes, for example, usage in spec parameter cells, test parameters, port exit conditions, reference level setup, and waveform timing setup.

The tools of the enVision++ executive system **130** include the operator tool **160**, the test tool **166**, the flow tool **164**, the waveform tool **170**, the spec tool **168**, the microflow tool **171**, and the method tool **172**. The tools include programs necessary to build a usable test program, tools a device engineer needs to tune and perfect the test program, tools that communicate results of tests to the operator, and other types of tools.

The spec tool **168** is a testing tool that allows a test engineer to tune and perfect a test program. The spec tool **168** is used to define parameters and expressions made up of parameters. The parameters are organized into categories that can be selected by a flow object. The parameters can be used in other objects and test methods. As the device is tested in different categories (i.e., speed categories), the objects and test methods are not affected.

The waveform tool **170** is another type of testing tool. The waveform tool **170** defines the waveform and timing relationships in a test pattern. These relationships resolve each of the vector cycle formats from the test patterns. This is done for all unique test vector combinations before the test pattern can be run. Cycle formats may be built on a cycle-to-cycle basis across all signals of the device under test **50**, or they may be built hierarchically with groups of signals and over multiple cycles. Because multiple cycles are defined together, the error checking can test for cycle-to-cycle timing violations. The software handles mapping the on-screen drawn waveforms onto the specific tester **10** hardware. The waveform tool **170** also reads a response log memory and displays the actual waveform at as it was seen by comparators of tester **10**.

Operator tool **160**, flow tool **164**, test tool **166**, method tool **172**, microflow tool **171**, and launcher **134** are described in more detail below.

FIG. **7** illustrates the graphical user interface for enVision++ launcher **134**. enVision++ launcher **134** allows the user of the electronic tester **10** to launch the enVision++ operating environment **130**. The user uses mouse **49** to click on the launch button **138** to launch the enVision++ executive system on network interface computer **14**. The graphical user interface **134** shown in FIG. **7** is the interface that appears to the user viewing the cathode ray tube **46** of network interface computer **14**.

Menu box **200** shows which software release of enVision++ is being launched by network interface computer **14**. The user can click with mouse **49** on user mode buttons **202** to indicate whether the enVision++ is in the production mode or the engineer mode. The user can indicate that a simulator mode is being used by using menu box **204**. Buttons **206** allow the user to indicate which test head of electronic tester **10** is being used for the embodiment of tester **10** with two test heads. By typing on line **208**, the user can indicate an operator tool option. The cancel button **210** allows the user to cancel the current use of launcher **134**, which results in the display of graphical user interface **134** being closed.

FIG. **8** illustrates the graphical user interface for operator tool **160** of enVision++ executive system **130**. Operator tool **160** allows the user of the electronic tester **10** to specify the test program to load. Operator tool **160** also allows the user to specify the flow and load board object to use. The test program can be executed from operator tool **160**, and indicators as to program status, and loop or single execute mode are available. Bin results go to a separate tool called the bin tool (not shown) and are not shown directly on the operator tool **160**. The bin tool shows which bin a DUT **50** goes into after failing a test.

The user can start a test program by clicking with mouse **49** on the start button **162**. The user can reset by clicking on button **236**. The user can restart a test program by clicking on button **238**.

The electronic test engineer who is using electronic tester **10** can specify the program name in line **220** of operator tool **160**. The path name for the program specified in line **220** is set forth in area **224**.

On line **222** the user can select an execution mode to run on a single pass, loop continuously, or loop until some condition is met. Lines **226** of operator tool **160** allow test option parameters to be displayed and altered. Those test option parameters are global to the test program. Lines **226** include allow the display of lot summary information and wafer displays. When the user pulls down the File menu **245** and clicks mouse **49** on the "Load" command, the fields within area **226** are filled in by the test program. Summary button **240** can be used to display how many devices were tested, how many failed, etc.

The pull down menu **248** called "Tools" allows the start-up by the user of any other test tools of the enVision++ executive system **130**.

The setup pull down menu **244** allows the user to establish the setup of function keys on the tester interface computer **14**. The setup **244** pull down menu also allows the user to specify the tester hardware initialization and specify the prober/handler set up.

Operator tool **160** allows protection to prevent unauthorized access to the tools that allow modification of a test program. Controls **234** allow the turning off and on of the break, trace, and override features. When the break button is turned on, the testing stops at break points.

The user can select button **242** for specifying operator variables. The operator variables are the variables that the production operator of electronic tester **10** can control. The test temperature is an example of an operator variable.

Operator tool **160** provides a common way to start both digital test programs and analog test programs. Operator tool **160** allows the user to load enVision++ executive digital test programs for testing the device under test **50**. The operator tool **160** also allows the user to load Cadence source and binary file formats for analog testing of the device under test **50**. The programs that can be specified in line **220** include both digital and analog test programs. Thus, the user of electronic tester **10** sees a common graphical user interface in the form of operator tool **160** when he or she wants to start a test program by pressing the start button **162**.

Button **230** of operator tool **160** allows the user to turn on or turn off the data log for the Cadence operating system for analog testing. When the datalog for the Cadence operating system is turned on, the measurements made during analog testing of DUT **50** are written to a file. Button **232** of operator tool **160** allows the user of the electronic tester **10** to turn on or turn off a data list for the Cadence operating system for analog testing of device under test **50**. The data list is similar to the data log, except that the data list takes the binary measurement information and puts that information in a format more understandable to the user of electronic tester **10**.

Button number **228** of operator tool **160** allows the user to turn on or turn off the enVision++ data log. When the enVision data log is turned on, the measurements made during digital testing of DUT **50** are written to a file.

Area **239** of operator tool **160** is used to display status. For example, the status may be that the program is loading.

FIG. **9** shows the icon palette **260** for displaying test method icons and the Cadence procedure icon. A test method is a procedural function written in C++ developed to perform a certain test or class of tests on the device under test **50**. Icon palette **260** shows the icons for the test methods **187**. These test methods **187** are complete and designed with necessary debug and characterization options.

The library of test methods includes opens and shorts ("OSpins"), power supply opens and shorts ("OSpower"), input leakage ("Itest"), output leakage ("Itest"), tristate leakage ("Itest"), current measurement ("Imeas"), functional test ("Ftest"), dynamic input voltages ("PARtest"), dynamic output voltages ("Vtest"), dynamic output currents ("Itest"), power supply margin ("PARtest"), timing verification ("PARtest"), static supply current ("Ptest"), dynamic supply

current ("Ptest"), supply current measurement ("Pmeas"), capacitance ("Ctest, Cmeas"), resistance ("Rtest, Rmeas"), voltage match ("Vmatch"), voltage differences ("Vdiff"), current match ("Imatch"), frequency ("FRQtest, FRQmeas"), and parameter match ("PARmatch").

Icon palette **260** includes a display mode **262** pull down menu for choosing the test methods **187** as the display. Icon palette **260** includes a line **264** for specifying the type of test method.

Line **266** of icon palette **260** allows the user to choose a Cadence procedure for display. The Cadence procedures are used for analog testing of DUT **50**. Clicking mouse **49** on the Cadence procedure line **266** causes icon palette **260** to display a Cadence procedure icon.

Controls **268** allow the user to choose a test method. Controls **270** allow the user to keep the selection, use a cloned test, or show the icons for the test methods. Controls **272** allow the user to empty the flow node, empty the test, empty a bin, or empty text. Button **274** allows the user to cancel the display of the icon palette.

Area **275** displays status.

FIG. **10** shows the graphical user interface for flow tool **164**. Flow tool **164** provides a graphical representation of program flow. The graphical representation of program flow is similar to a flow chart for software. Flow tool interface **164** includes display portion **322** for displaying program flow. The program flow displayed is the sequence of operation of the overall program. Each node in the flow display **322** may be a test, a bin, an entry point, or a subflow identifier.

Tests are selected from the Cadence procedures (for analog tests) and the library **187** of test methods (for digital tests). The library may also be extended by the user with user additions **189**. The test flow may be developed hierarchically by means of subflows.

The test node may have a simple two-way output based on past/fail, or have a multiple way output decision based on the results of the test. Each output is represented on the flow with a port designator. The decision that causes this port to be traversed is defined by test tool **166**.

Display **322** of flow tool **164** shows a demonstration display that includes digital test methods **331** through **343**. Display **322** also shows icons **344** and **345** for Cadence procedures for doing analog testing of DUT **50**. Cadence procedures are written in the Cadence language. Cadence procedure **344** is an AC/DC test with respect to DUT **50**. Cadence procedure **345** is a process array analog test with respect to DUT **50**. As shown in FIG. **10**, the various test methods and Cadence procedures shown in display **322** are linked by lines showing program flow.

The program flow shown in display area **322** can be altered graphically by a user by using mouse **49**. Altering the program flow in display **322** in turns alters the actual program flow. In other words, a user of electronic tester **10** can use mouse **49** to rearrange icons, add and delete icons, rearrange lines of program flow, and add and delete lines of program flow in display **322**, which in turn alters the actual program flow.

Line **300** of flow tool **164** allows the user to specify what program flow the user wishes to have displayed. Menu **302** allows the user to specify entry subflows. Buttons **308** allow the user to specify on start, on reset, on initial flow, on load, on restart, on power down, and user calculation.

Buttons **310** allow the user to specify whether the following items should be turned on and off: break, trace, override, and datalog. Line **312** allows the user to specify subflow. Button **314** allows the user to specify the viewing of graphics. Button **316** allows the user to specify the count. Button **318** allows the user to display an expression. Button **320** allows the user to specify the move option that allows the user to move from area to area within display **322**.

Button **304** allows the user to begin a test by clicking on button **304**. Button **306** is a reset button.

When a user clicks mouse **49** on an icon of display **322**, text or a formula associated with that icon appears in area **313**. In addition, if the user uses the pull down menu called view **323** to display information, such as the length of a test, that information is displayed in area **313**. Area **301** is used to display status.

FIG. **11** shows the graphical user interface for test tool **166**. Test tool **166** is a testing tool that a test engineer uses to develop and fine tune a test program. Test tool **166** provides the user with specific details of each test.

Test tool **166** provides an interface with respect to both the digital C++ test methods and the Cadence procedures for analog testing.

Test tool **166** allows the user to specify the setup and exit conditions that are to be stored in a particular test object. The setup and exit conditions are used whenever a test flow (as determined by the flow object) requires that a test be executed.

Line **360** of test tool **166** allows the user to specify a test. Button **362** allows the user to begin the test. Button **364** allows the user to reset the test. Buttons **366** allow the user to specify whether the following controls should be turned on or off: break, trace, datalog, and override.

Button **368** allows the user to set up a loop for looping a test method or Cadence procedure. Button **370** allows the user to halt the looping of a test method or Cadence procedure. For one embodiment, button **372** allows the user to specify an analysis of the test method or Cadence procedure. For one embodiment, button **374** allows the user to characterize the test method or the Cadence procedure. For one alternative embodiment, button **372** allows the user to specify an analysis of a test method but not a Cadence procedure, and button **374** allows the user to characterize a test method but not a Cadence procedure.

Display **380** specifies the test method or Cadence procedure that is being analyzed by the test tool **166**. Display **382** of test tool **166** displays the spec/mask objects defining the parameters to be used.

Display **384** displays the entry objects. The entry objects, which are also called the setup objects, are to be loaded prior to execution of the particular test method or Cadence procedure. Display **386** displays the exit objects. Upon completion of the test method or Cadence procedure, the exit objects are loaded to establish the appropriate reset or idle state for the device under test **50**. All tester **10** functions that are not specified in either the set-up or entry objects will be left unchanged.

Clicking on a test method icon or a Cadence procedure icon allows the user to select the display of the source code associated with the test method or the Cadence procedure.

Area **388** of test tool graphical user interface **166** is a separate area for the definition of the input and output parameters of the test method or Cadence procedure. The names and types of these parameters are defined by the test method or Cadence procedure. These parameters may be either constant values (for example, 5.25 volts), parameter values directly from the spec object (for example, Vcc), or

expressions made up of constants and parameter values (for example, (Vcc−10%)+500 millivolts).

Area **371** is used to display information requested by using the pull down menu called view **421**. Area **371** also has other uses. If the user clicks mouse **49** on one of the cells or boxes within display area **388**, the full text associated with that cell appears in area **371**. If the user indicates a cell within display area **388** by using mouse **49** and then writes test in area **371**, then hitting the return key causes that text to be written to the respective cell within display area **388**.

Clicking on move button **378** with mouse **49** causes the displaying of arrows that allow a user to move from cell to cell within display area **388**.

Button **376** toggles between "expression" and "value." When "expression" is selected using button **376**, a formula is shown in the respective cell selected within area **388**. When "value" is selected using button **376**, a result of that formula—i.e., a value—is shown in the respective cell selected within area **388**.

Button **372** is used for controlling debugging. Button **374** is used for controlling the characterization options with respect to the test method or Cadence procedure.

Area **390** of test tool graphical user interface **166** is for exit port expressions. Test tool **166** defines the exit port expressions. A list of expressions is evaluated in sequence. When a true condition is encountered, the associated port will be chosen. The exit ports are not part of the test method or Cadence procedure. Decisions are generally based on a pass/fail flag from the test method (or Cadence procedure) or based on comparisons to measurements on the DUT **50**.

FIG. **12** shows how to call a Cadence procedure (for analog testing) from the test tool **166**. Test tool **166** includes a test tool "find" function **400**. The test tool "find" window **400** can be displayed by choosing the "find" function from the options pull-down menu **420**.

When the test tool find window **400** is chosen using the options pull down menu **420**, the test tool find window **400** appears on the cathode ray tube **46** of network interface computer **14**. The test tool find window **400** allows the user to locate test methods by pressing button **404** or locate Cadence routines by pressing button **402**. In FIG. **12**, the Cadence routines button **402** was selected. The names of the Cadence modules are displayed in area **406**. A Cadence module is a file. There can be multiple Cadence procedures within a Cadence module. The Cadence routines are displayed in area **408** of test tool find window **400**. The selected object is displayed on line **410** of test tool find window **400**. The user can click on button **412** to indicate that the Cadence routine specified should be displayed and called. The user can cancel the display of the test tool find window **400** by pressing button **414**.

For one embodiment, Cadence routines lack the following features associated with digital test methods: multisite support, analysis support, characterization support, help/documentation, and argument comments. Moreover, for that embodiment, the Cadence routines have not been designed and tested to be general. For an alternative embodiment, Cadence procedures include multisite support, analysis support, characterization support, help/documentation, argument comments, and have been designed and tested to be general.

FIG. **13** shows the graphical user interface for the editor and debugger compiler **136** for the network interface computer **14**. The editor and debugger compiler **136** is also called Cadence debugger **136**.

Cadence is a full featured line-by-line compiled test language designed specifically for writing and debugging of Cadence procedures for analog testing of device under test **50**.

The Cadence debugger **136** helps to eliminate the time consuming edit/compile/link/restart process. With the Cadence debugger **136**, the test engineer can stop at any line in the Cadence test program, change any line of code, and continue debugging.

The Cadence debugger **136** is supported by tools that guide the test engineer through the development process, including instrumentation syntax, a library of DSP functions, graphical status displays, instrument control panels, and DSP waveform displays.

The Cadence debugger graphical user interface **136** appears on the screen **46** of network interface computer when the test engineer clicks mouse **49** on a Cadence procedure icon or object, such as Cadence procedure icon **344** shown in FIG. **10**. The Cadence debugger **136** shown in FIG. **13** then appears on screen **46** of network interface computer **14**, which allows the test engineer to view, debug, or execute the Cadence test procedure.

Pull down menus **432** on the Cadence debugger **136** allow the test engineer to choose various options regarding file, edit, search, keys, panel, tester, data list, data log, and tools.

Area **434** of graphical user interface **136** displays the Cadence source code, which allows the user to edit, debug, or simply view the source code.

Triggers and break points are supported by the Cadence debugger **136**. Triggers and break points serve multiple purposes on electronic test system **10**. One application is to provide a mechanism for debugging a test program. A second application is to provide a mechanism for analyzing or debugging device under test **50**. A third application is to provide a means of collecting (or disabling collection of) data from device under test **50**. All of these uses are also supported by the operator tool **160** of FIG. **8**, which includes trigger and break point tools found in pull down menu **248** and break button **234**.

The user of electronics tester **10** may select from a variety of trigger events, and upon the event occurring, may either suspend execution or perform some operation to continue. Triggers and break points can be enabled and disabled as needed.

The execution panel **435** of Cadence debugger **136** allows the user of test system **10** to call enVision++ test methods and other routines. One way is to execute an enVision++ object. One function call can execute nearly any enVision++ object. Another way is by executing an enVision++ ETIC. "ETIC" stands for enVision ++ tester interface class. An ETIC is the interface between enVision ++ and the hardware of electronic tester **10**. ETICs are built into the Cadence operating system and are called in a Cadence like syntax. The other way is to get the value of an enVision++ expression. In short, Cadence and enVision ++ can share data and can communicate with each other. For one embodiment, enVision ++ test methods, routines, and data can be called from Cadence only if both enVision ++ and Cadence are loaded.

The run button **436** of Cadence debugger graphical user interface **36** shown in FIG. **13** causes the Cadence source code to execute. Resume button **438** causes the Cadence source code to resume execution. Step button **440** allows the test engineer to step through a Cadence routine. Button **442** of Cadence debugger **136** allows the test engineer to set a break point for the Cadence source code.

Button **444** of Cadence debugger **136** allows the test engineer to execute a single line at time of the Cadence source code. Button **446** of Cadence debugger allows the test engineer to run the Cadence program up to a specific line.

Button **448** allows the user to resume to a line. Button **450** allows the test engineer to let the Cadence program execute through a specific break point. Button **452** allows the test engineer to delete a break point. Button **454** allows the test engineer to move a pointer. Button **456** allows the user to view other panels. Button **458** allows the user to resume to the end body. Button **460** allows the user to delete all break points. Button **462** allows the user to view an active line. Button **464** allows the user to view the device tool. Button **466** allows the user to view a block diagram. Button **468** allows the user to view a control panel. Button **470** allows the user to set a DT break point. Button **472** allows the user to update.

Area **474** of Cadence debugger is an echo-back panel that displays text or status. Area **475** of Cadence debugger **136** is a command line for the user to execute commands with respect to execution panel **435**.

FIG. **14** shows a portion of the microflow tool graphical user interface **171** of electronic tester **10** that demonstrates that Cadence routines can be called from the enVision++ microflow tool **171**. Microflow tool **171** is the interface between the user and a microflow object and is the user's view into the microflow object. This provides testing capabilities that are useful during the debug of each microflow.

A test engineer writes a microflow object when the test engineer wants to deviate from a test method. A microflow object can be called from a test method, such as from one of test methods **187**. The microflow object is invoked to perform the additional functions that the test engineer wants that are not provided by the test method.

To view microflow objects, the user of electronic tester **10** can launch the microflow tool **171** from the tools menu **248** of operator tool **160**. For the user to actually test the device under test **50** in the context of a single test, the user starts microflow tool **171** by examining one of the microflow object icons in test tool **166**.

During the debug phase of a test program, the microflow tool **171** is used to trace the low-level hardware functions calls executed by the test/microflow objects up to the break point, and to reexecute that sequence after manual changes are made by the user. For the latter, the microflow tool **171** can be used to perform temporary changes, or to support the debug of the test program or device under test **50**.

Controls **490** of microflow tool **171** allow the user to select the file, edit, view, and options pull-down menus. Display area **492** shows the name of the microflow object being displayed. Area **493** is used to display information selected from the view menu of area **490**, or to display and alter text with respect to a cell from area **494**.

Not shown in FIG. **14** are the buttons for execute, value, and move controls for microflow tool **171**. Also not shown in FIG. **14** is a help menu for microflow tool **171**.

Display area **494** of microflow tool **171** allows the display of information with respect to the microflow object, including tag, enable, value, and event.

Window **496** for finding a microflow event can be displayed by using the pull down menu of the options command **490** of microflow tool **171**. Button **498** allows the user to select built in events. Button **500** allows the user to choose microflow events. Button **506** allows the user to select levels objects. Button **502** allows the selection of microflow objects.

Button **504** allows the user to select Cadence routines.

Area **508** allows the display of names of modules. Area **510** allows the display of names of routines. In FIG. **14**, the Cadence routines are selected and the names of the Cadence routines are shown in area **510**.

Area **512** allows the display of a selected object. Button **514** allows the user to agree to the finding of a particular microflow event. A button **516** allows the user to cancel the finding of a particular microflow event.

FIG. **15** shows a portion of the method tool graphical user interface **172**. Method tool **172** is used for viewing, modifying, creating, or debugging test methods, user functions, data log formatting routines, microflow event methods, or external interface methods. Pull-down menus **520** allow the user to select file, edit, and options routines.

The test method that is subject of the method tool is set forth in line **522**. An icon for the test method is shown in box **536**. The revision information regarding the test method is shown in box **534**. The directory for the test method is specified in line **524**. The dynamically linked library ("DLL") file name is specified in line **526**. Button **538** is a button for unlinking the dynamic method. Button **528** is for editing sources. Button **538** is for reloading. The build button (not shown) will compile the source file to executable object file. Button **552** is for creating a test method. Entering a command in line **530** and pressing move button **532** allows the user to move to another portion of the enVision++ executive system **130** and out of method tool **172**. Area **540** of the method tool graphical user interface of method tool **172** shows information regarding the method tool such as argument definition.

Cadence procedures can be selected from within the method tool graphical user interface **172**. The select Cadence window **542** that can called from method tool **172** allows a user to select a Cadence module.

The select Cadence window **542** is useful because Cadence modules can be called from C++ test method. The method tool **172** is useful for developing C++ test methods. If a Cadence module is to be called from a test method, the select Cadence window **542** is useful in selecting which Cadence procedure to call.

To select a Cadence module, the user clicks mouse **49** on the edit pull-down menu **521** and chooses the Cadence modules command. The result of this is that window **542** appears on CRT **46** of network interface computer **14**. Area **544** of window **542** lists the names of the Cadence modules that can be selected. The user can select a Cadence module by highlighting the module with mouse **49** and by hitting OK button **546**. To cancel a selection of a Cadence module, the user hits the cancel **548** button with mouse **49**.

If the Cadence module is selected by hitting OK button **546**, then method tool **172** automatically generates the code to allow a test method written in C++ to call a Cadence module. The test engineer can then select the callable Cadence procedures from within the Cadence module.

FIG. **16** shows the architecture of the electronic tester **10** with respect to the action bus™ **600**. Action bus **600** is also referred to as marker bus **600**. Action bus **600** allows the synchronization of events among all the instructions for precision control of each test. Action bus **600** allows the electronic tester **10** to have modular architecture. Modularity means that a test engineer can replace one part of electronic tester **10** and electronic tester **10** will still work.

Action bus **600** comprises action number bus **601** and action complete bus **602**. Action number bus **601** is used to send markers (also called action numbers or action time stamps) to initiate action by the modular circuitry within electronic tester **10**. Action number bus **601** is also referred to as action marker bus **601** and action timestamp bus **601**.

Action complete bus **602** sends action complete markers also called action complete numbers, action complete time stamps, or acknowledgements that indicate to the modular circuitry that the action requested has been completed. Action complete bus **602** is also called action complete number bus **602** or action complete time stamp bus **602**. For one embodiment, action number bus **601** is **16** bits wide and action complete bus **602** is one bit wide.

Action number bus **601** is coupled to digital pattern generator **606**, digital pattern generator **608**, source and measure sequencers **611** of sequenced measure system ("SMS") **610**, and pacemaker **92** of tester controller **90**. Pacemaker **92** is in turn coupled to local processor **613** of DC source/measure instrument **612** via bus **604**.

Action complete bus **602** is coupled to digital pattern generator **606**, digital pattern generator **608**, and source and measured sequencers **611** of sequenced measure system **610**.

Bidirectional flag line **614** is coupled between digital pattern generator **606** and tester controller **90**. Bidirectional flag line **616** is coupled between digital pattern generator **608** and tester controller **90**.

Digital pattern generator **606** is a custom processor that acts as a sequencer. Digital pattern generator **606** is used to generate digital test vectors for testing device under test **50**. Digital pattern generator **606** can drive 1,024 pins of the device under test **50** in parallel. Digital pattern generator **606** thus generates digital test vectors for digital testing of a device under test **50**. Digital pattern generator **606** is microcoded and includes assembly code executed by clock steps. Test engineers write the digital test vectors in order to test device under test **50**. Digital pattern generator **606** is clocked by a clock generator.

Digital pattern generator **608** is similar to digital pattern generator **606**. Digital pattern generator **608** is used to send digital test vectors to the device under test **50** but sends those digital test vectors to different pins of the device under test than digital pattern generator **606**. Digital pattern generator **606** and **608** can send test vectors at different times to different pins of device under test **50**.

Sequenced measure system **610** includes source and measure sequencers **611**. Sequenced measure system **610** is used for analog testing of the device under test **50**. The sequenced measure system **610** is controlled by pacemaker **92**, which in turn is controlled by tester controller **90**.

The sequenced measure system **610** is the DSP source and measurement system of electronic tester **10**. Sequenced measure system **610** provides test capability for audio, video, datacom, and telecom type devices under test **50**.

For one embodiment, the sequenced measure system **610** features analog performance from DC to 100 megahertz and local DSP processing that eliminates data transfer through the tester **10**. One high speed version of sequenced measure system **610** contains analog circuitry optimized for analog waveform operations up to 100 megahertz. That high speed version is intended for applications such as MPEG video devices, high speed data converters, and DVD read channels.

For an alternative embodiment, a high resolution version of sequenced measure system **610** uses analog circuitry optimized for lower frequency and higher precision operations. The high resolution version of sequenced measure system **610** is suited for applications such as audio circuits, high resolution data converters, ISDN, and ADSL. The sequenced measure system **610** includes a event processor and a controller/processor. Sequenced measure system **610** is clocked.

DC source/measure unit **612** is used for DC source and measure with respect to device under test **50**. The DC source and measure operations done by DC source/measure unit **612** are analog tests with respect to device under test **50**. DC source/measure unit **612** includes a local processor **613**. DC source/measure unit **612** is controlled by pacemaker **92**, which in turn is controlled by tester controller **90**. For an alternative embodiment, DC source/measure unit **612** is directly connected to action bus **600**.

Digital pattern generators **606** and **608** communicate with tester controller **90** via respective bidirectional flag lines **614** and **616**. For example, digital pattern generators **606** and **608** can use bidirectional flag lines **614** and **616** to interrupt. Tester controller likewise can send signals to digital pattern generator **606** and **608** via bidirectional flag lines **614** and **616**. For example, tester controller **90** can use bidirectional flag lines **614** and **616** to request the digital pattern generators **606** and **608** to start generating patterns.

The action number bus **601** works as follows. A test engineer places up to 4,096 markers in a digital pattern produced by digital pattern generator **606** to mark specific actions that need to occur elsewhere in tester **10**. Each marker causes digital pattern generator **606** to send a marker over action number bus **610** to sequenced measure system **610** and pacemaker **92**. Digital pattern generator **606** can also be used to place markers in a pattern where analog events need to occur by importing mixed mode patterns from automated program generation tools. Such mixed mode patterns contain flags indicating that analog events are to occur.

Digital pattern generator **608** can also send out markers on action number bus **601** at appropriate times to cause SMS **610** and pacemaker **92** to initiate action.

When a marker appears on action number bus **601**, pacemaker **92** can respond to the marker by sending a signal on line **604** to initiate action by DC source/measure unit **612**.

Digital pattern generator **606** can be the master at times. As bus master, digital pattern generator **606** can send markers over action number bus **601** to source and measure sequencers **611** and pacemaker **92**. Digital pattern generator **608** can also receive a marker from action number bus **601** in response to digital pattern generator **606** sending out such a marker. Thus, digital pattern generator **608** can be a slave. At other times, digital pattern generator **608** can be the bus master and send out markers to source and measure sequencers **611**, pacemaker **92**, and digital pattern generator **606**.

For one embodiment, source and measure sequencers **611**, DC source/measure unit **612**, and pacemaker **92** are always slaves and never the masters with respect to markers on action number bus **601**. For alternative embodiments, source and measure sequencers **611**, DC source/measure unit **612**, and pacemaker **92** can be masters and send markers on action number bus **601** to digital pattern generators **606** and **608** and to other circuitry coupled to action number bus **601**.

An example illustrates how action number bus **601** works. A test engineer working on electronic tester **10** may, for example, want to send a DC source of 5 volts to the device under test **50** at 500 milliseconds into a test. The test engineer puts a command in digital pattern generator **606** for digital pattern generator **606** to send out a marker on action number bus **601** when the 500 millisecond point has been reached with respect to the generation of test vectors by digital pattern generator **606**. For this example, digital pattern generator **606** is acting as the master with respect to the action number bus **601**. The digital pattern generator **606** puts a marker on action number bus **601** when the 500

millisecond point is reached. Pacemaker **92** receives the marker at this point and sends a command over line **604** to prompt the local processor **613** to cause the DC source/measure unit **612** to set the DC source with respect to a pin on the device under test **50** to 5 volts. Sequenced measure system **610** would also see the marker placed by digital pattern generator **606** on action number bus **601** and perform a source test at that same point with respect to another pin of the device under test **50**.

Accordingly, it should be appreciated that the action bus **600** arrangement allows the sequenced measure system **610** and the DC source/measure unit **612** to act locally. The digital pattern generator **606** can simply trigger action that will be done by the sequenced measure system **610** and the DC source/measurement unit **612**. This allows the electronic tester **10** to in effect think globally and act locally.

For an alternative embodiment of the invention, a pulsed power source (described in more detail below) can also be coupled as a slave to action bus **600**.

For an alternative embodiment, a power voltage/current ("PVI") unit can also be coupled as a slave to action bus **600** via pacemaker **92** and line **604**. For yet another alternative embodiment, a PVI unit is directly connected to action bus **600**.

When sequenced measure system **610** receives a marker from action number bus **601**, sequenced measure system **610** knows what actions to take with respect to analog testing of device under test **50**. Sequenced measure system **610** has processing circuitry that triggers particular tests in response to the receipt of markers from action number bus **601**. Likewise, DC source/measure unit **612** also knows what particular actions to take when it receives a prompting from pacemaker **92** triggered by pacemaker **92** receiving a marker on action number bus **601**.

The source and measure sequencers **611** of sequenced measure system **610** can send an action complete marker over action complete bus **602** to digital pattern generator **606** or digital pattern generator **608** indicating that a particular action requested has been completed. Digital pattern generators **606** and **608** can also send an action complete marker from the slave to the master acknowledging the completion of a task by a slave. Indeed, any slave with respect to action bus **600** can send action complete markers over action complete bus **602**.

For one embodiment of the present invention, a marker on action number bus **601** appears as the binary number 01011. For one embodiment, the compiler for digital pattern generators **606** and **608** compiles that pattern as a "DUT_ ready" command. For that embodiment, a "DUT_ready" command is written in the source code for digital pattern generators **606** or **608** at appropriate points where the test engineer wishes a marker to be sent on action number bus **601** to trigger action by a slave, such as the SMS **610**.

As an example, if digital pattern generator **606** sends out a marker at a "DUT_gready" command, the sequenced measure system **610** starts a source sequence of color bar measurement with respect to DUT **50** when the marker is received by sequenced measure system **610**. As another example, the marker may trigger the DC source/measure unit **612** to measure a pin of device under test **50** and put the measurement into a results array on a pin list.

As discussed above, electronic tester **10** includes both circuitry for doing digital testing of DUT **50** and circuitry for doing analog testing of DUT **50**. The discussion below in connection with FIGS. **17–21** describes the digital test circuitry in more detail. The discussion below in connection with FIGS. **22** and **23** discusses certain analog test circuitry in more detail.

FIG. **17** shows digital subsystems **650** for testing the device under test **50** in a digital manner. Digital subsystem **650** includes control pattern processing unit **652**; data pattern processing unit **674**; pattern select processing unit **660**; waveform, timing, and formatter unit **668**; and pin electronics cards **64**.

Digital subsystem testing unit **650** is coupled to the device under test **50**. Pin electronics cards **64** are located in test head **16** and coupled to device under test **50**. For an alternative embodiment, pin electronics cards **64** are also coupled to a second device under test coupled to a second test head **18**. The rest of digital subsystem testing unit **650** besides pin electronics **64** resides within digital circuitry **20** (shown in FIG. **1**) and digital resources **94** (shown in FIG. **3**). The entire digital subsystem **650** resides within digital boards **64** (shown in FIG. **4**).

Control pattern processing unit **652** shown in FIG. **17** includes control pattern memory address generator **654** and control pattern memory **656**. Control pattern memory is coupled to the DSP and analog systems **658** (for example, SMS **610**) via action bus **600** (see FIG. **16**). DSP and analog systems unit **658** are in turn coupled to the device under test **50**. For an alternative embodiment, DSP and analog systems **658** are also coupled to another device under test in second test head **18**.

For one embodiment of the invention, control pattern processing unit **652** acts as the digital pattern generators **606** and **608** of FIG. **16**.

For one embodiment, digital test subsystem **650** is controlled by the enVision++ executive system **130** of network interface computer **14**.

For digital testing of device under test **50**, test patterns can be contained in two types of vector memories—namely, control pattern memory **656** or data pattern memory **676**. During pattern execution, either one or both of data pattern memory **676** and control pattern memory **656** may be used to generate the data pattern. Dynamic selection of the pattern source, (i.e., either data pattern memory **656** or control pattern memory **656**) for each tester channel is performed on a vector by vector basis by pattern select circuitry **666**. For one embodiment, pattern select circuitry **666** can also select algorithmic pattern generator **665** dynamically for each tester channel on a vector-by-vector basis.

Data pattern processing unit **674** includes data pattern memory address generator **678** and data pattern memory **676**. Pattern select unit **660** is coupled to both data pattern processing unit **674** and control pattern processing unit **652**. Pattern select unit **660** is in turn coupled to waveform, timing, and formatter unit **668**. Waveform, timing and formatter unit **668** is in turn coupled to pin electronics **64**, which in turn are coupled to device under test **50**.

Pattern select unit **660** includes pattern select circuitry **666**, which is coupled to DSP send unit **662**, scan PG unit **664**, and algorithmic pattern generator ("APG") **665**. Pattern select circuitry **666** is also coupled to control pattern memory **656** and data pattern memory **676**. Pattern select circuitry **666** sends its output to waveform, timing, and formatter unit **668**.

Waveform, timing, and formatter unit **668** includes waveform memory **670** and timing generators and formatters unit **672**.

Pattern select circuitry **666** and waveform, timing and formatter unit **668** operate on an independent per pin basis with respect to device under test **50** and provide independent per pin functions.

Pattern select circuitry **666** sends to waveform memory **670** the appropriate pattern to be applied to waveform

memory **670**. Waveform memory **670** in turn sends the pattern information to the timing generators and formatters unit **672** which generates the proper timing and formatting for sending the signals to the pin electronics unit **64** and in turn to the device under test **50**.

One embodiment of electronic tester **10** provides up to a 250 megahertz non-multiplexed input/output data rate on each individual channel and offers a non-multiplexed 500 megahertz input/output data rate capability with constrained formatting options. An alternative embodiment of electronics tester **10** provides up to 125 megahertz input/output data rates. All data rates are doubled in the multiplexed mode.

FIG. **18** illustrates control pattern processing unit **652**, which includes control pattern memory address generator **654** and control pattern memory **656**. Control pattern memory **656** includes control pattern memory sequence microinstructions **690**, pin vector data **692**, per-pin opcode **694**, data pattern memory control information **696**, algorithmic pattern generator microinstructions **698**, and action bus marker information **700**.

Control pattern processing unit **652** features microinstructions that control the pattern sequence of control pattern memory **656** as well as providing master control of other system resources. The microinstructions **690** and per pin opcode **694** of control pattern memory **656** provide flexible control of over all test pattern execution, including synchronizing vector flow with the data pattern processing unit **674**.

The control pattern memory address generator **654** provides addressing to the control pattern memory **656** and steps the control pattern memory **656** through addresses. In particular the control pattern memory address generator **654** steps through the control pattern memory sequence microinstructions **690** and executes them. The control pattern memory sequence microinstructions **690** are used to generate complex pattern sequences that require looping, conditioning, branching, and nested subroutines.

Per pin opcode **694** provides control over per-pin pattern source selection. DPM control information **696** provides control over DPM sequencing. APG microinstructions **698** provide control over algorithmic pattern generator algorithms.

Control pattern memory **656** also includes action bus markers **700**. The action bus markers **700** are sent out at various points during the control pattern memory sequence of microinstructions **690**. The action bus markers **700** are sent out on action number bus **601** of action bus **600** shown in FIG. **16**.

For one embodiment, the control pattern processing unit **652** includes 16 levels of nested subroutines and four 16 bit loop counters. For one embodiment, control pattern processing unit **652** can perform conditional branching and conditional subroutine calls and returns. For one embodiment, control pattern processing unit **652** includes a 16 bit vector repeat counter. For one embodiment, control pattern processing unit **652** can perform sequential match operations. One embodiment, DPM control information **696** includes data pattern memory address, load, and step instructions.

For one embodiment of the invention, control pattern processing unit **652** controls whether or not the vector waveform selection comes from control pattern memory **656** or data pattern memory **676**.

The standard control pattern memory **656** vector depth is 32K for one embodiment and 16K for another embodiment. Control pattern memory microinstructions can be executed on every vector when running a test pattern in an extended waveforms mode for one embodiment. In the high frequency format embodiment, control pattern memory microinstructions can be executed on every other vector. For one embodiment, in the extended waveforms mode, pin vector data **692** is 16K by 3 bits per pin. For another embodiment, in the high frequency format, pin vector data **692** is 32K by one bit per pin.

FIG. **19** illustrates data pattern processing unit **674**. Data pattern processing unit **674** includes data pattern memory address generator **678** and data pattern memory **676**. Data pattern memory **676** includes vector repeat count information **702** and pin vector data **700**.

Data pattern memory address generator **678** receives set and step instructions from the control pattern memory **656**. The data pattern memory address generator **678** sends addresses to the vector repeat count portion **702** of data pattern memory **676** in order to step through information in data pattern memory **676**. Data pattern memory address generator **678** can receive information from data pattern memory **676**.

Data pattern processing unit **674** provides long sequential vector patterns with vector repeat capabilities, which allows test engineers to simulate digitally intensive devices. Each data pattern memory **676** vector location can specify a repeat count of up to 2,047 cycles. Maximum data pattern memory **676** size depends on the configuration and frequency mode of electronic test system **10**.

Returning to FIG. **17**, during pattern execution, either the data pattern memory **656** or the control pattern memory **676**, or both, may be used to generate the data pattern to be applied to device under test **50**. For each tester channel, the pattern select unit **660** will perform dynamic selection of the pattern source from either the control pattern memory **656**, the data pattern memory **676**, or the algorithmic pattern generator **665** on a vector-by-vector basis.

The vectors from the control pattern memory **656** and data pattern memory **676** include a waveform selection address for the waveform select memory **670** for each pin of the DUT **50**. For one embodiment, the waveform select memory **670** for each pin is 32k by 8 bits. A control pattern **656** instruction is used to specify whether the data pattern memory **676** or the control pattern memory **656** is to be used for providing this address. The "SWCDPM" control pattern memory **656** instruction selects the data pattern memory **676** as the source for the waveform memory **670** address, effective on the cycle executed. The "SWCCPM" instruction selects the control pattern memory **656** as the source for the waveform memory **670** address effective on the cycle executed.

FIG. **20** shows algorithmic pattern generator ("APG") **665** coupled to CPM unit **652** and pattern source select **666**. APG **665** produces digital patterns for testing embedded memory arrays. APG **665** derives its control from CPM unit **652**. This allows memory test algorithms to be interspersed with the logic vectors required for accessing embedded memory of DUT **50**.

APG can be used for testing embedded memories as well as memory chips.

APG **665** features per pin architecture, which allows a test engineer to configure for "virtual" APG fields. The test engineer can create a relatively wide range of memory test patterns, including march, surround/disturb, and galloping rows/columns. The test engineer can assign any APG **665** signal to any tester channel of electronic tester **10**. For one embodiment, APG **665** instructions can be executed up to 250 Megahertz.

APG **665** includes signal select circuitry **667**, initial value register **659**, foreground register **661**, background register

657, and gate 663. The APG instruction codes include modifiers 669 with respect to foreground register 661 and background and register 657. The modifier instructions 669 are sent from CPM unit 652 to APG 665. The modifier instructions 669 include incrementing and decrementing the foreground register 661; loading the contents of the initial value register 659 into foreground register 661; swapping the contents of the foreground and background registers 661 and 657; shifting the contents of foreground register 661 left and right; and shifting the contents of foreground register 661 and adding zeroes and ones. Control logic (not shown) of APG 665 carries out the modifier instructions 669 received from CPM unit 652.

APG 665 includes gate 663 for providing logical operations between foreground register 661 and background register 657. The APG instruction codes include source select instructions 671, which include an "AND" operation with respect to the contents of the foreground and background registers 661 and 657; an "OR" operation with respect to the contents of the foreground and background registers 661 and 657; selection of an inverse of the contents of foreground register 661; and selection of either foreground register 661 or background register 657. Signal select circuitry 667 of APG 665 controls the selection of signals from foreground register 661, background register 657, and gate 663 in response to the source select instructions 671 sent from CPM unit 652.

FIG. 21 is a block diagram of the fail log memory ("FLM") 701 used in conjunction with the algorithmic pattern generator 665 to test embedded memories in system-on-a-chip ICs, for example. The FLM 701 will record failures that occur during the testing of the embedded memory of DUT 50 and will record the location of failing cells in the memory array of DUT 50. This failure information is then exported for the purposes of repairing the IC in the event that redundant memory cells are available.

FLM 701 can be used to test embedded memories as well as memory chips.

The device under test 50 is connected through the per-pin compare logic to input matrix 709 that establishes a data connection to the cell fail memory 711, the row fail memory 713, and the column fail memory 715. Simultaneously, the APG 665 provides addressing information through programmable pipeline 705 to the fail memories 711, 713, and 715, and to an address fail log memory 707. A local processor acts as a bit map scanner 717 to organize the fail information into a compressed electronic form for export to the memory repair process. For one embodiment, the bit map scanner 717 includes a Power PC 750 CPU sold by Motorola Corporation of Schaumburg, Ill. Bitmap processor 717 allows for bitmaps and redundancy analysis.

For one embodiment, FLM 701 helps to ensure real-time accumulation of memory array bit map information at rates up to 250 megahertz. The FLM 701 supports an accumulate mode and a mask mode.

The accumulate mode stores DUT 50 memory array errors in the FLM 701 at the same locations as the DUT 50 array addressed by APG 665. APG 665 generates an address that is sent to both DUT 50 and FLM 701. This address goes through a programmable pipeline before it reaches FLM 701 to allow for DUT 50 designs with pipelined address/data. If the CPM 652 microcode contains an FLM 701 log instruction and a channel error exists on any FLM 701 channel, the system accesses the FLM 701 cell memory 711 to see if that memory location has had a previously recorded error. If not, the system records the error in cell memory 711 and records the address in the address fail log memory 707.

The mask mode enables the execution of a test pattern using errors previously accumulated or loaded into FLM 701 to mask out any subsequent errors at those locations in the DUT 50 memory array.

FIG. 22 is a block diagram of sequenced measure system ("SMS") 610. Sequenced measure system 610 provides the analog source and measure functions with respect to device under test 50. In other words, sequenced measure system 610 is one of the analog testing circuits with respect to device under test 50. SMS 610 sends and receives analog signals with respect to DUT 50. Sequenced measure system 610 is located within analog circuitry 22 of electronic tester 10 (shown in FIG. 1), within analog resources 96 (shown in FIG. 3), and within analog boards 62 (shown in FIG. 4).

Sequence measure system 610 operates cycle by cycle and is controlled by event processor 710, the controller/processor 712, and tester controller 90.

Sequence measure system 610 is coupled to action bus 600, which is in turn coupled to the digital pattern generators 602 and 608 and tester pacemaker 92 of tester controller 90. Sequenced measure system 610 is also coupled to tester controller 90.

Sequenced measure system 610 includes an event processor 710 for initiating analog tests upon receipt of a marker on action number bus 601 of action bus 600. Action number bus 601 and action complete bus 602 of action bus 600 are coupled to event processor 710.

Event processor 710 is in turn coupled to source sequencer 726 and measure sequencer 730. Upon receiving a marker from action number bus 601 of action bus 600, event processor 710 sends signals to either the source sequencer 726 or the measure sequencer 730 to begin a sequence of either source or measure tests with respect to device under test 50. Source sequencer 726, measure sequencer 730, and event processor 710 together comprise the source and measure sequencers 611 shown in FIG. 16.

Source sequencer 726 of FIG. 22 is coupled to sequencer memory 728 which includes microcode for performing source style analog tests with respect to device under test 50. Measure sequencer 730 is coupled to sequencer memory 732. Sequencer memory 732 includes microcode for guiding measure sequencer 730 through analog tests with respect to device under test 50.

Source sequencer 726 is also coupled to source waveform memory 734 containing waveforms with respect to the analog tests with respect to device under test 50. Measure sequencer 730 is coupled to measure waveform memory 736 for performing measure analog tests with respect to device under test 50.

Controller/processor 712 of sequenced measure system 610 oversees and controls the source and measure analog tests performed by the sequence measure system 610 and also performs local analysis of measured data. The controller/processor 712 is in turn coupled to tester controller 90 which controls controller/processor 712.

Controller/processor 712 is coupled to the source waveform memory 734 and the measure waveform memory 736. Controller/processor 712 controls the source waveform memory 734 and the measure waveform 736 with respect to the reading and writing of waveform data with respect to device under test 50. An output of source waveform memory 734 is coupled to an input of digital-to-analog conversion circuitry 738. The output of digital-to-analog conversion circuitry 738 is coupled to filters ranging circuitry 742.

An output of filters ranging circuitry 744 is coupled to an input of analog-to-digital conversion circuitry 740. An out-

put of analog-to-digital conversion circuitry **740** is coupled to an input of measure waveform memory **736**.

Multiplexer **714** is coupled to clock divider circuitry **720**. Clock divider circuitry **720** is coupled to source waveform memory **734** and source sequencer **726**. Multiplexer **714** is coupled to device under test **50** and clock lines **752** and **754**. Multiplexer **714** is also coupled to multiplexer **716** and **718**.

Multiplexer **718** is coupled to clock divider unit **724**, which is in turn coupled to measure waveform memory **736**. Multiplexer **716** is coupled to clock divider circuitry **722**, which in turn is coupled to measure sequencer **730**. Multiplexers **714**, **716**, and **718** each have inputs coupled to device under test **50**.

FIG. **23** is a block diagram of pulse power source ("PPS") **770** of electronic tester **10**. Pulse power source **770** is coupled to action number bus **601** and action complete bus **602** of action bus **600**. PPS is also coupled to DUT **50**. Pulse power source **770** is a multichannel high-power voltage/current source designed to test the smart power blocks on a system-on-a-chip IC. Pulse power source circuitry **770** is thus used for analog testing of device under test **50**.

Pulse power system **770** resides within analog circuitry **22** and test head **16** (shown in FIG. **1**). Pulse power circuitry **770** also resides within analog board **62** and test head **16** shown in FIG. **4**. Pulse power circuitry **770** also resides in analog resources **96**, test head interface **98**, and test head **16** (shown in FIG. **3**).

Pulse power source **770** shown in FIG. **23** includes pulse power source controller **772**, which is coupled to action bus **600**. Power pulse controller **772** includes a Power PC CPU microprocessor **778** sold by Motorola Corporation of Phoenix, Ariz. Power pulse source controller **772** also includes a sequencer **780** with 32 channels.

The pulse power source sequencer **780** is in turn coupled to rail power module **774**, which in turn is coupled to test head module **776**. Test head module **776** is coupled to the device under test **50**.

Pulse power source sequencer **780** sends **32** channels of data and control information to rail power module **774**. Rail power module **774** includes pulse power source rail power units covering all **32** channels, including rail power unit **782** covering channels one to four and rail power unit **784** covering channels twenty-nine to thirty-two shown in FIG. **23**. Rail power module **774** in turn sends data, control, and power signals to test head module **776**. Test head module **776** includes pulse power source test head units for all 32 channels, including test head unit **786** (for channels **1–4**) and test head unit **788** (for channels **29–32**) shown in FIG. **23**. Test head module **776** in turn sends per channel HF, HS, LS, and LF signals to device under test **50**.

Under the control of pulse power source sequencer **780**, each pulse power source channel can produce voltages up to 100 volts or currents up to 10 amps for one embodiment, providing timing resolution of one microsecond on any event across all channels.

The pulse power source **770** sends signals to test head **16** resident power amplifiers that provide the bandwidth necessary to handle device transients and produce pulsed load waveforms. The pulse power source sequencer **780** is programmable, which enables the test engineer to program the output values of all amplifiers and determine the timing relationship between consecutive values on any number of channels or the relative timing between channels.

Pulse power sequencer **780** also allows the test engineer to place measure strobes relative to any forced value across all channels and make single or multiple measurements on any number of channels. These features enable parallel measurement of multi-output devices and digitizing of any power waveform that can then be analyzed using DSP math functions.

Controller **772** of PPS **770** is coupled to action bus **600**. Controller **772** can be triggered to measure the current at a point in the digital pattern when controller **772** receives a marker over action number bus **601** of action bus **600** sent by either digital pattern generator **606** or digital pattern generator **608**. This allows full characterization of power usage.

FIG. **24** shows the clocking architecture of electronic test system **10**. Digital pattern generator **606** is coupled to digital pins **802** which in turn are coupled to device under test **50**. Digital pattern generator **608** is coupled to digital pins **804**, which in turn are coupled to device under test **50**. Digital pattern generators **606** and **608** generate the digital test patterns for device under test **50**. Sequenced measure system **610** performs the sequence source and measure analog tests with respect to device under test **50**. Sequenced measure system **610** is coupled to DUT **50**. Sequenced measure system **610** includes a source circuitry **820** and measure circuitry **818**. Source circuitry **820** includes multiplexer **714**, divider **720**, source sequencer **726**, sequencer memory **728**, source waveform memory **734**, and event processor **710** (shown in FIG. **22**). Measure circuitry **818** includes multiplexers **732**, measure waveform **736**, and event processor **710** (shown in FIG. **22**).

Wideband sampler **816** shown in FIG. **24** is coupled to the SMS **610**. Wideband sampler **816**, which is coupled to DUT **50**, provides a high bandwidth interface to device under test **50** for any of the DSP or time measure instruments in the tester.

Fixed low frequency clock source **809** provides a global clock source for electronic test system **10**. Clock source **809** is also referred to as the system-wide frequency reference clock source **809** or the reference clock source **809**.

The low frequency clock source **809** has a frequency on the order of approximately 10 megahertz.

Fixed low frequency clock source **809** is in turn coupled to a variable frequency reference clock source **34** that is coupled to digital pattern generators **606** and **608**. Each of the digital pattern generators **606** and **608** has its own clock source that is generated in response to the variable clock source **34**.

Digital pattern generator **606** has its own local clock source **806** that runs at approximately 100 megahertz. The relatively high speed clock **806** is coupled to variable frequency clock source **34** and is derived from variable low frequency clock source **34** by multiplying the frequency of the variable speed clock source **34**. Likewise, digital pattern generator **608** includes a local high-speed clock source **808** that is coupled to variable frequency clock source **34** and is derived from clock source **34** by multiplying the frequency of clock source **34**. The local high-speed clock source **808** runs at approximately 100 megahertz.

Even though local clocks **806** and **808** typically can run at up to 100 megahertz, those local high speed clock sources **806** and **808** can be varied by varying the frequency of variable clock source **34**.

Thus the fact that variable frequency clock source **34** can be varied means that the local clocks **806** and **808** are likewise varied by varying the frequency of clock source **34**. In other words, the fact that the clock source **34** can be varied to different frequencies means that the local clock

sources **806** and **808** can likewise be varied. Given that the local clock sources **806** and **808** are derived by multiplying the frequency of low speed clock source **34**, that means that a broad range of frequencies can be generated by clock sources **34**, **806**, and **808**.

For one embodiment, the frequencies of high speed clocks **806** and **808** can be derived from the variable speed clock by multiplying the frequency of clock **34** by fractions. Thus, for that embodiment, the frequencies of the high speed clocks **806** and **808** would be greater than the frequency of clock **34**. For an alternative embodiment, the frequencies of clocks **806** and **808** are derived from clock **34** by multiplying the frequency of clock **34** by numbers greater than one. For that alternative embodiment, the frequencies of clocks **806** and **808** would be greater than the frequency of clock **34**.

The user of electronic tester **10** can use network interface computer **10** to adjust the clock frequency of variable clock generator **34**, which in turn adjusts the frequencies of clocks **806** and **808**.

Each digital pattern generator **606** and **608** can operate at an independent data rate while using the system-wide frequency reference clock source **809**. This allows the test engineer to run two functional patterns in parallel at different speeds. In addition, every digital pin of digital pins **802** and **804** contains a non-harmonically related clock that can change frequency on a vector-by-vector basis and continue running between patterns in order to keep alive circuits on device under test **50**, such as on-board phase lock loops or switched capacitor filters that cannot be left idle between tests.

Analog clocks **810** and **812** provide clocking for the sequenced measure system **610**, wide band sampler **816**, and arbitrary waveform source **814**, which are used for analog testing of DUT **50**. Analog clock **812** is coupled to arbitrary waveform source **814** and wideband sampler **816**. Analog clock **810** is coupled to sequenced measure system **610** and wideband sampler **816**.

For one embodiment, analog clocks **810** and **812** are independent analog master clocks that drive all of the DSP instruments in electronic tester **10** with frequencies from 100 megahertz up to 2.4 gigahertz. This clocking flexibility allows the test engineer to create any clocking relationship required to implement techniques such as coherent undersampling of high speed waveforms. In addition, these multiple high-resolution clock sources **810** and **812** allow the test engineer to set up undersampling applications with many effective sampling rates.

Analog clock **810** and **812** are coupled to fixed clock reference **809**. Analog clocks **810** and **812** derive their frequencies by multiplying the frequency of global clock **809**.

Arbitrary waveform source **814** can sample arbitrary waveforms at speeds up to 2.4 Giga-samples/second with analog bandwidths in excess of one gigahertz. The arbitrary waveform source **814** can provide DSP based waveform generation capability. Arbitrary waveform source **814** is coupled to device under test **50**.

For one embodiment of the present invention, variable frequency clock source **34** is a frequency synthesizer model PTS 310D sold by Programmed Test Sources of Littleton, Mass. The design of the internal circuitry of variable frequency clock source **34** itself is not, however, intended to be part of the present invention.

FIG. **25** is a block diagram of arbitrary waveform source **814**, which is used to perform analog tests with respect to device under test **50**. Arbitrary waveform source **814** is used for applications such as hard disk drive or high-speed datacom applications, which require high-speed arbitrary waveforms. Arbitrary waveform source **814** can also be used to generate sine waves or multitones for general DSP applications, such as analog to digital converters and analog filter testing. Arbitrary waveform source **814** features synchronization to a digital pattern, output ranging, and differential outputs. For one embodiment, arbitrary waveform source **814** resides within (1) analog circuitry **22** and test head **16** shown in FIG. **1**; (2) analog resources **96**, test head interfaces **98** and **100**, and test heads **16** and **18** shown in FIG. **3**; and (3) analog boards **62** and test head **16** shown in FIG. **4**.

As shown in FIG. **25**, the fixed frequency reference **809** provides inputs to analog master clock **812** and internal clock **854** of arbitrary waveform source **814**. Internal clock **854** derives a clock of 2.4 gigahertz from the fixed frequency reference **809**. Analog master clock **812** derives a clock frequency of 100 megahertz to 2.4 gigahertz from fixed clock source **809**. Both clocks **812** and **854** send clock signals to clock control circuitry **852**, which includes source select and dividers.

Arbitrary waveform source includes a waveform control sequencer **856**, a waveform sequence memory **858**, waveform memories **860** and **862**, digital to analog converters **864** and **866**, clocked combiner **868** for analog multiplexing, and output conditioning circuitry **870** that includes an offset, a filter, and gain circuitry. The output conditioning circuitry **870** is coupled to device under test **50**.

Digital pattern control in the form of gate/triggers and branch vectors are sent to waveform sequencer **856**. The waveform sequencer **856** sends addresses to waveform memories **860** and **862**. Waveform memories **860** and **862** send data to the digital-to-analog converters **864** and **866**. The digital analog converters **864** and **866** send analog information to the analog multiplexing clocked combiner **868**, which in turn sends signals to output conditioning circuitry **870**, which in turn sends signals to the device under test **50**.

Waveform control sequencer **856** also sends segment gain, offset, and filter settings to output conditioning circuitry **870**. Waveform sequence memory **858** provides data to waveform control sequencer **856** at addresses specified by sequencer **856**. Microcode for the waveform control sequencer **856** is stored in waveform sequence memory **858**.

FIG. **26** shows wideband sampler **816**, which is clocked by analog clock **812**. Wideband sampler **816** provides a high bandwidth interface to device under test **50** for any DSP or time measurement instruments in electronic tester **10**. The wideband sampler **816** is thus used for analog testing of DUT **50**. The wideband sampler **816** is used for applications such as graphics devices or datacom transmitters for wideband time domain measurements of parameters such as rise time and settling time. The wideband sampler **816** can also be used to complement the arbitrary waveform source **814** as a DSP digitizer front end.

For one embodiment, wideband sampler **816** is located in test head **16** of electronic tester **10**.

Wideband sampler **816** can capture signals with bandwidths up to one gigahertz and edges with rise times under 100 picoseconds. Wideband sampler **816** includes an operational amplifier **890** with an input coupled device under test **50**. The output of operational amplifier **890** is coupled to bridge **894**. Bridge **894** is in turn coupled to sampled output operational amplifier **892**.

Thus, a single platform electronic tester **10** has been described that can test digital integrated circuits, analog

integrated circuits, mixed signal integrated circuits and system-on-a-chip integrated circuits.

In the foregoing specification, the invention has been described with reference to specific exemplary embodiments thereof. It will, however, be evident that various modifications and changes made be made thereto without departing from the broader spirit and scope of the invention as set forth in the appended claims. The specification and drawings are, accordingly, to be regarded in an illustrative rather than a restrictive sense.

What is claimed is:

1. An electronic tester, comprising:

a test head to couple to a device under test, wherein the device under test can be system-on-a-chip integrated circuit, a mixed signal integrated circuit, a digital integrated circuit, or an analog integrated circuit;

digital test circuitry that applies digital test signals to the device under test coupled to the test head and receives digital outputs from the device under test in response to the digital test signals;

analog test circuitry that applies analog test signals to the device under test coupled to the test head and receives analog outputs from the device under test in response to the analog test signals;

memory test circuitry that applies memory test patterns to the device under test coupled to the test head and receives memory outputs from the device under test in response to the memory test patterns;

a tester computer that supervises the application of digital, analog, and memory test signals from the digital test circuitry, analog test circuitry, and memory test circuitry to the device under test such that signals applied to the device under test can be solely digital test signals, solely analog test signals, solely memory test signals, or mixed digital, analog, and memory test signals, wherein the test head, the digital test circuitry, the analog test circuitry, the memory test circuitry, and the tester computer are operable as a single platform, wherein the digital test signals, the analog test signals, and the memory test patterns can be applied serially or concurrently to the device under test.

2. The electronic tester of claim 1, wherein the memory test circuitry comprises an algorithmic pattern generator.

3. The electronic tester of claim 2, wherein the memory test circuitry further comprises a fail log memory.

4. The electronic tester of claim 1, wherein the digital test circuitry comprises a control pattern memory processing unit and a data pattern memory processing unit.

5. The electronic tester of claim 1, wherein the analog test circuitry comprises a sequenced measure system.

6. The electronic tester of claim 5, wherein the analog test circuitry further comprises vector radio frequency circuitry.

7. The electronic tester of claim 1, wherein the analog test circuitry comprises a pulsed power source.

8. The electronic tester of claim 1, wherein the digital test circuitry, the analog test circuitry, and the memory test circuitry are modular and reconfigurable.

9. An electronic tester, comprising:

means for applying digital test signals to a device under test and receiving digital outputs from the device under test in response to the digital test signals;

means for applying analog test signals to the device under test and receiving analog outputs from the device under test in response to the analog test signals;

means for applying memory test patterns to the device under test and receiving memory outputs from the device under test in response to the memory test patterns;

computing means for supervising the application of digital, analog, and memory test signals to the device under test by the means for applying digital test signals, analog test signals, and memory test patterns, wherein the device under test can be a system-on-a-chip integrated circuit, a mixed signal integrated circuit, a digital integrated circuit, an analog integrated circuit, or a memory integrated circuit, wherein the means for applying digital test signals, the means for applying analog test signals, the means for applying memory test patterns, and the computing means are coupled to a single platform, wherein the digital test signals, the analog test signals, and the memory test patterns can be applied serially or concurrently to the device under test.

10. An electronic tester, comprising:

analog test circuitry that applies analog test signals to a device under test coupled to a test head and receives analog outputs from the device under test in response to the analog test signals;

a tester controller that sends action packets to the analog test circuitry to select characteristics of analog tests to be performed by the analog test circuitry;

digital test circuitry that applies digital test signals to the device under test coupled to the test head and receives digital outputs from the device under test in response to the digital test signals;

memory test circuitry that applies memory test patterns to the device under test coupled to the test head and receives memory outputs from the device under test in response to the memory test patterns;

a computer coupled to the tester controller, the digital test circuitry, and the memory test circuitry, wherein the computer causes the tester controller to send action packets to the analog test circuitry to execute analog tests of the device under test, wherein the computer causes the digital test circuitry to execute digital tests of the device under test, and wherein the computer causes the memory test circuitry to execute memory tests with respect to the device under test, wherein the analog tests, the digital tests, and the memory tests can be applied serially or concurrently to the device under test.

11. A method for an electronic tester, comprising:

presenting to a user of the electronic tester a computer-generated graphical user interface for launching an operating system for the electronic tester, wherein the operating system can oversee selectable serial or concurrent execution of digital test programs, analog test programs, and memory test programs for testing a device under test coupled to the electronic tester;

launching the operating system in response to user input via the computer-generated graphical user interface.

* * * * *